

FOXCONN A75M02

FAB: 1.0

AMD FM1 APU + FCH HUDSON D2/D3 CHIPSET

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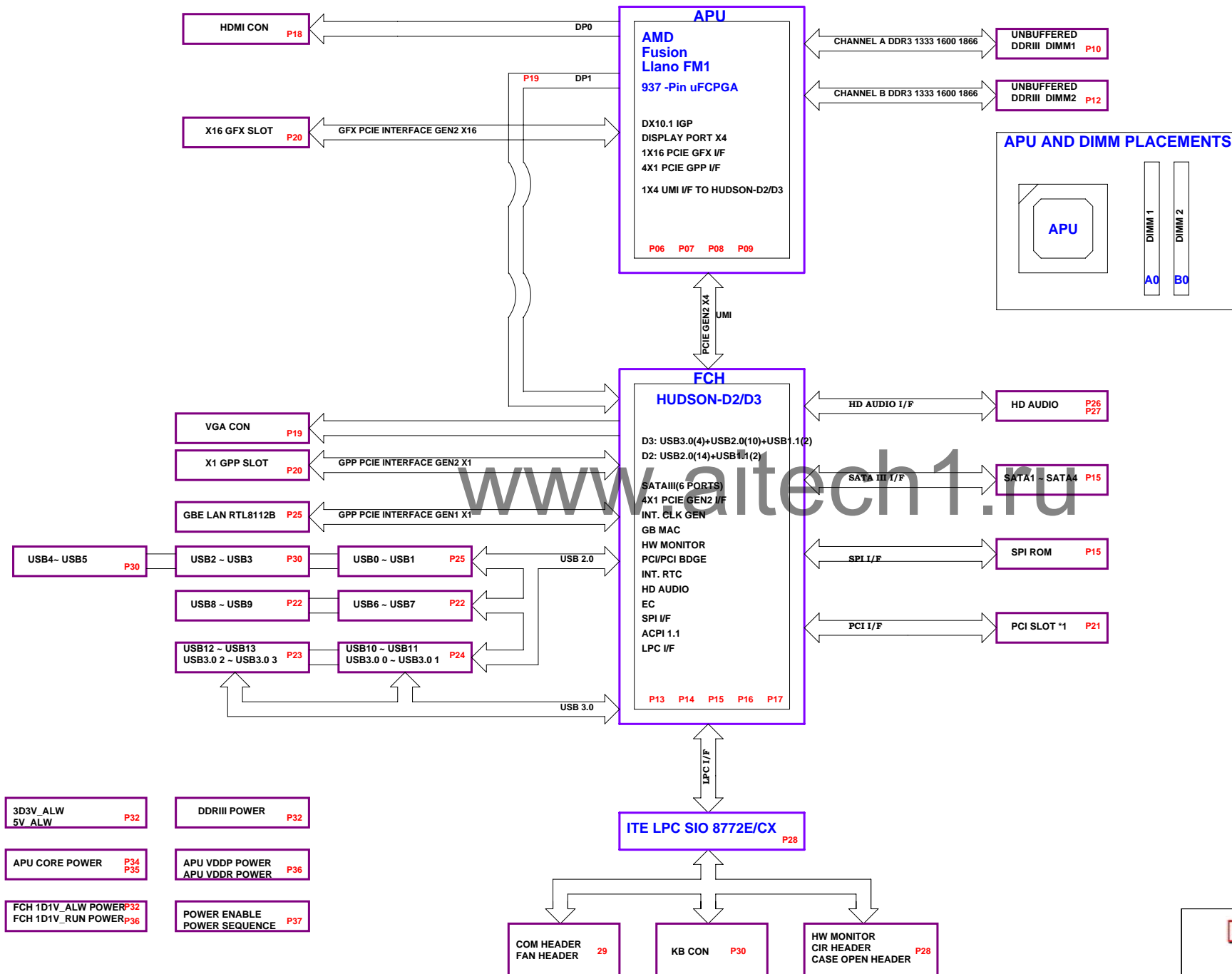
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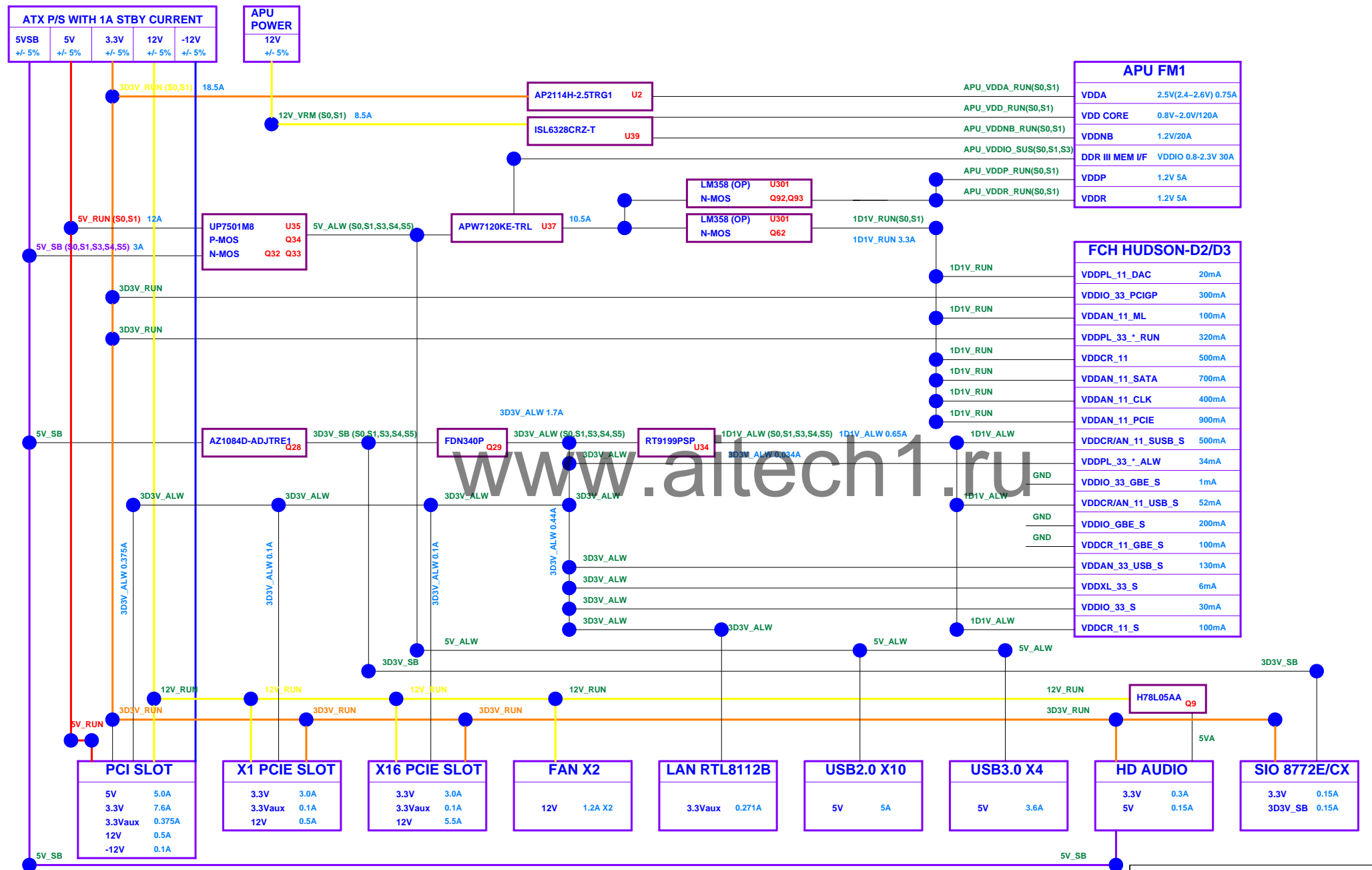
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A75M02 BLOCK DIAGRAM



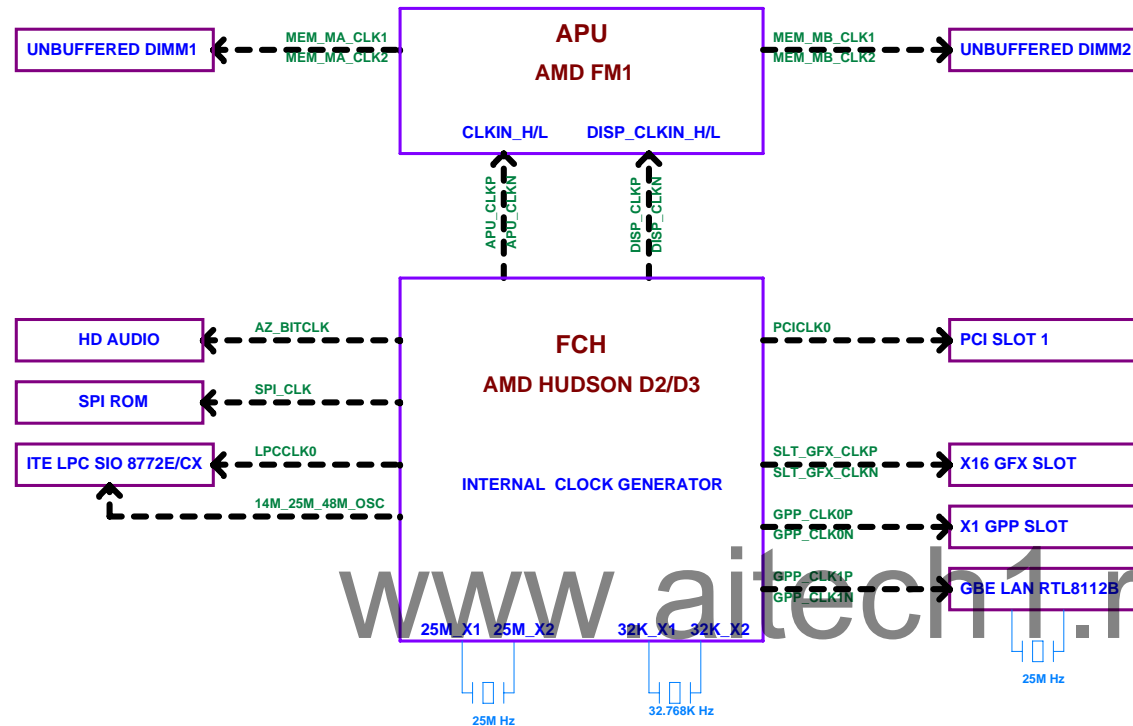
A75M02 POWER DELIVERY CHART



APU FM1	
VDDA	2.5V(2.4~2.6V) 0.7A
VDD CORE	0.8V~2.0V/120A
VDDNB	1.2V/20A
DDR III MEM V/F	VDDIO 0.8~2.3V 30A
VDDP	1.2V 5A
VDDR	1.2V 5A

FCH HUDSON-D2/D3	
VDDPL_11_DAC	20mA
VDDIO_33_PCIGP	300mA
VDDAN_11_ML	100mA
VDDPL_33_*_RUN	320mA
VDDCR_11	500mA
VDDAN_11_SATA	700mA
VDDAN_11_CLK	400mA
VDDAN_11_PCIE	900mA
VDDCR/AN_11_SUSB_S	500mA
VDDPL_33_*_ALW	34mA
VDDIO_33_GBE_S	1mA
VDDCR/AN_11_USB_S	52mA
VDDIO_GBE_S	200mA
VDDCR_11_GBE_S	100mA
VDDAN_33_USB_S	130mA
VDDXL_33_S	6mA
VDDIO_33_S	30mA
VDDCR_11_S	100mA

A75M02 INTERNAL CLOCK MODE



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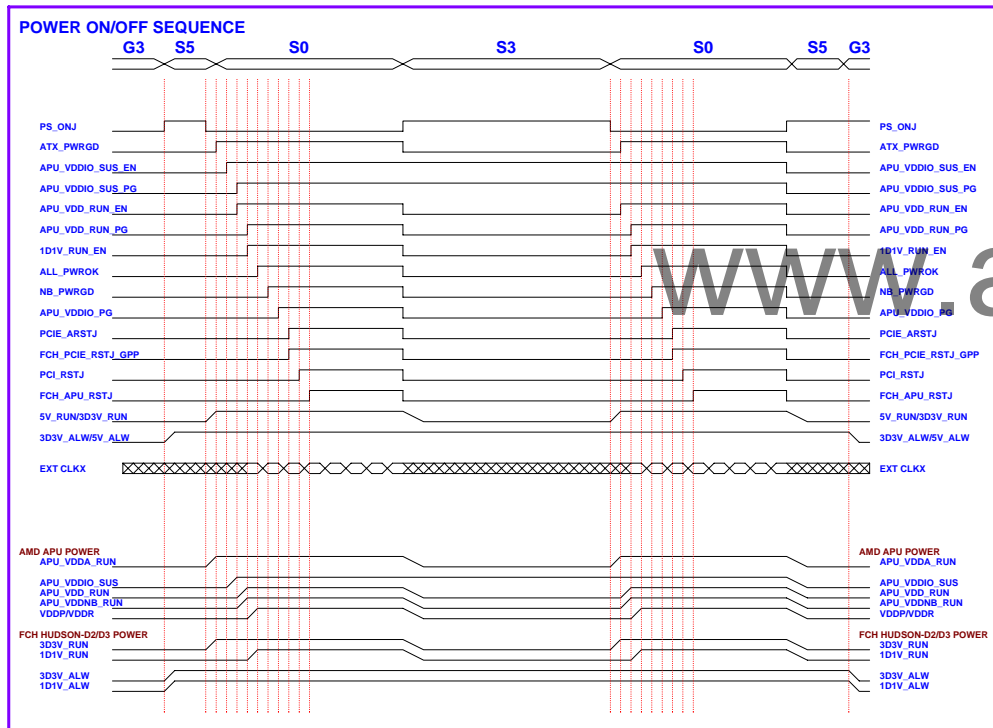
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CLOCK DISTRIBUTION			
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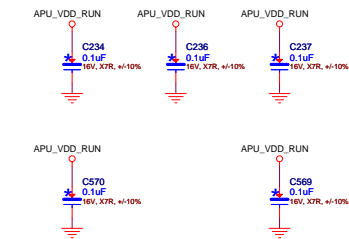
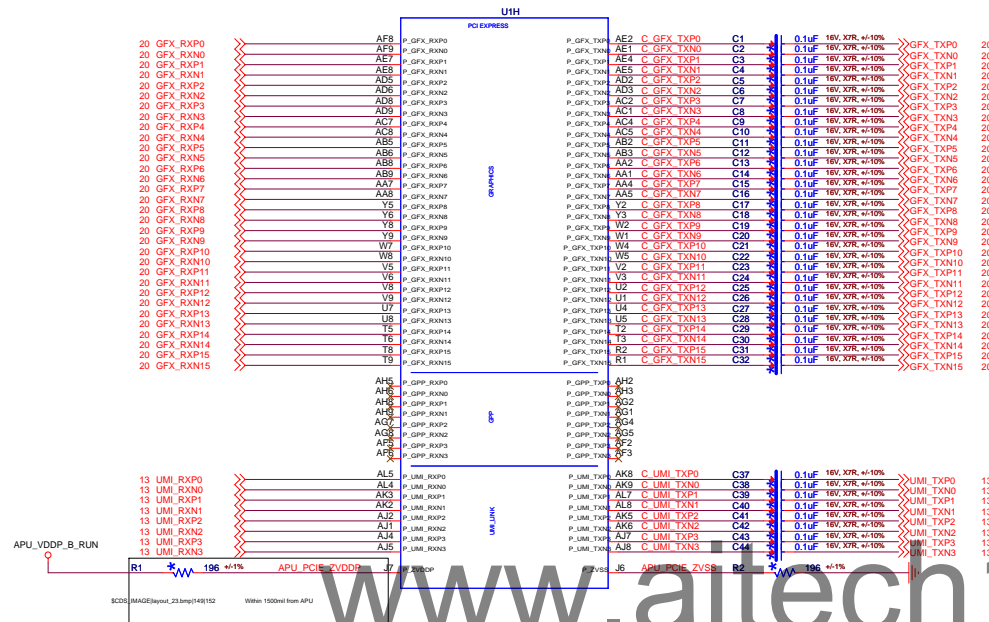
A75M02 MISC TABLES

POWER RAIL		S0	S1	S3	S4	S5	POWER RAIL		S0	S1	S3	S4	S5
12V_RUN	+12V	ON	ON	OFF	OFF	OFF	1D1V_RUN	+1.1V	ON	ON	OFF	OFF	OFF
12V_VRM	+12V	ON	ON	OFF	OFF	OFF	APU_VDD_RUN	SVI	ON	ON	OFF	OFF	OFF
N_12V_RUN	-12V	ON	ON	OFF	OFF	OFF	APU_VDDNB_RUN	SVI	ON	ON	OFF	OFF	OFF
5V_SB	+5V	ON	ON	ON	ON	ON	APU_VDDA_RUN	+2.5V	ON	ON	OFF	OFF	OFF
3D3V_SB	+3.3V	ON	ON	ON	ON	ON	APU_VDDIO_SUS	+1.5V	ON	ON	ON	OFF	OFF
5V_ALW	+5V	ON	ON	ON	ON	ON	APU_VTT_SUS	+0.75V	ON	ON	OFF	OFF	OFF
3D3V_ALW	+3.3V	ON	ON	ON	ON	ON	APU_VDDR_RUN	+1.2V	ON	ON	OFF	OFF	OFF
A_VBAT	+3.0V	ON	ON	ON	ON	ON	APU_VDDP_RUN	+1.2V	ON	ON	OFF	OFF	OFF
1D1V_ALW	+1.1V	ON	ON	ON	ON	ON							
5V_RUN	+5V	ON	ON	OFF	OFF	OFF							
3D3V_RUN	+3.3V	ON	ON	OFF	OFF	OFF							
5VA	+5V	ON	ON	OFF	OFF	OFF							

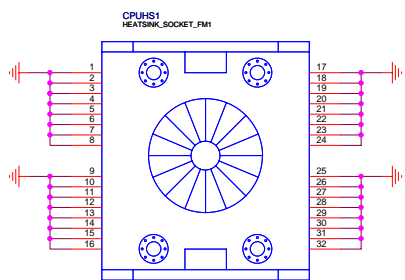
RESET TABLE		
SOURCE	SIGNAL NAME	LINKED DEVICES
FCH	PCIE_RST2J_GPP	GPP X1 SLOT/ LAN RTL8112B
	FCH_PCIE_RSTJ_GPP	GFX X16 SLOT
	PCIE_ARSTJ	LPC SIO 8772E/CX
	PCI_RSTJ	PCI SLOT 0
	FCH_APU_RSTJ	APU
APU	A_HDA_RSTJ	HD AUDIO CODEC ALC662/VT1705CE
APU	MEM_MA_RSTJ	DIMM1
APU	MEM_MB_RSTJ	DIMM2
PWR BTN	MASTER_RSTJ	FCH

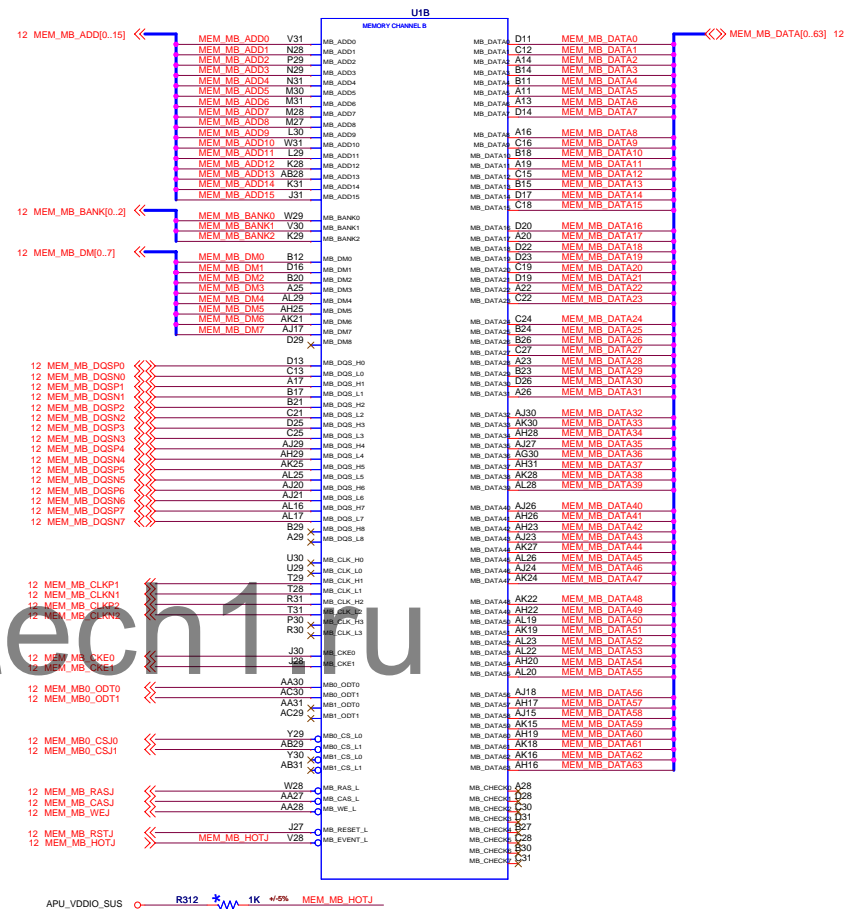
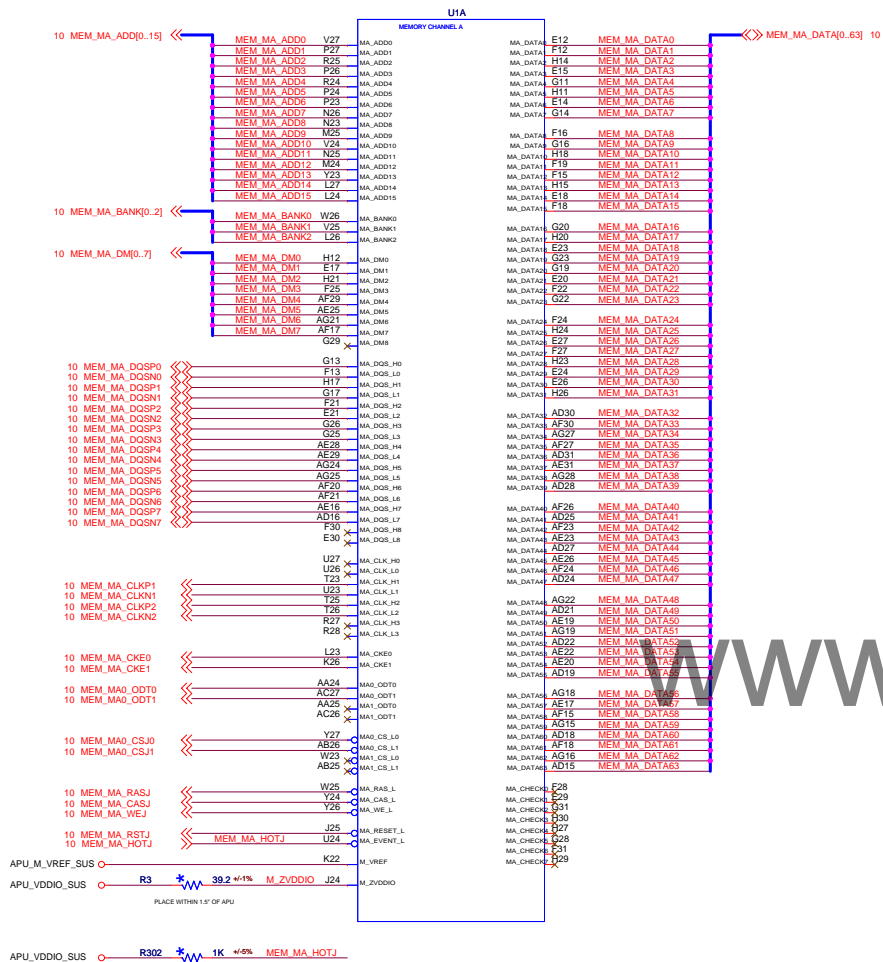
Explanation	
FCH	Fusion Controller Hub
UMI	Unified Media Interface



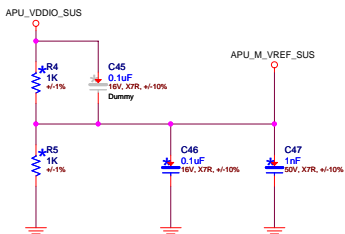


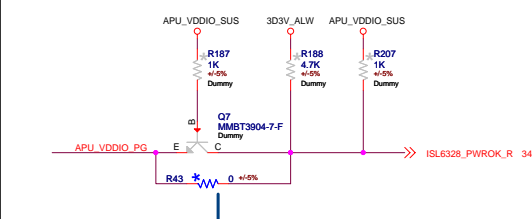
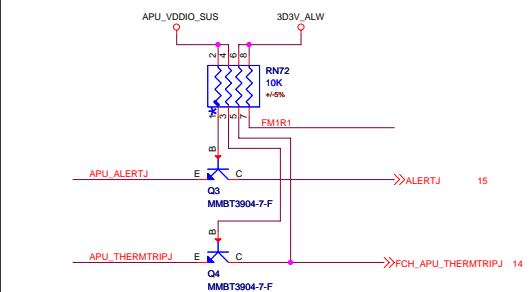
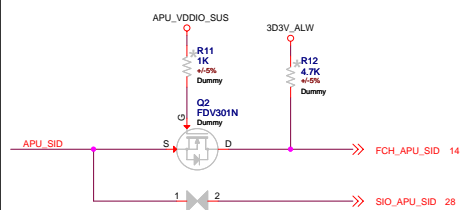
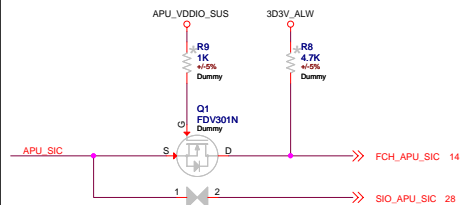
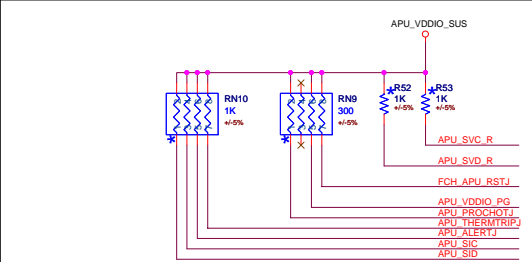
Place across each APU_VDD_RUN-GND plane seam



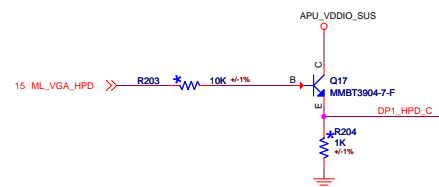
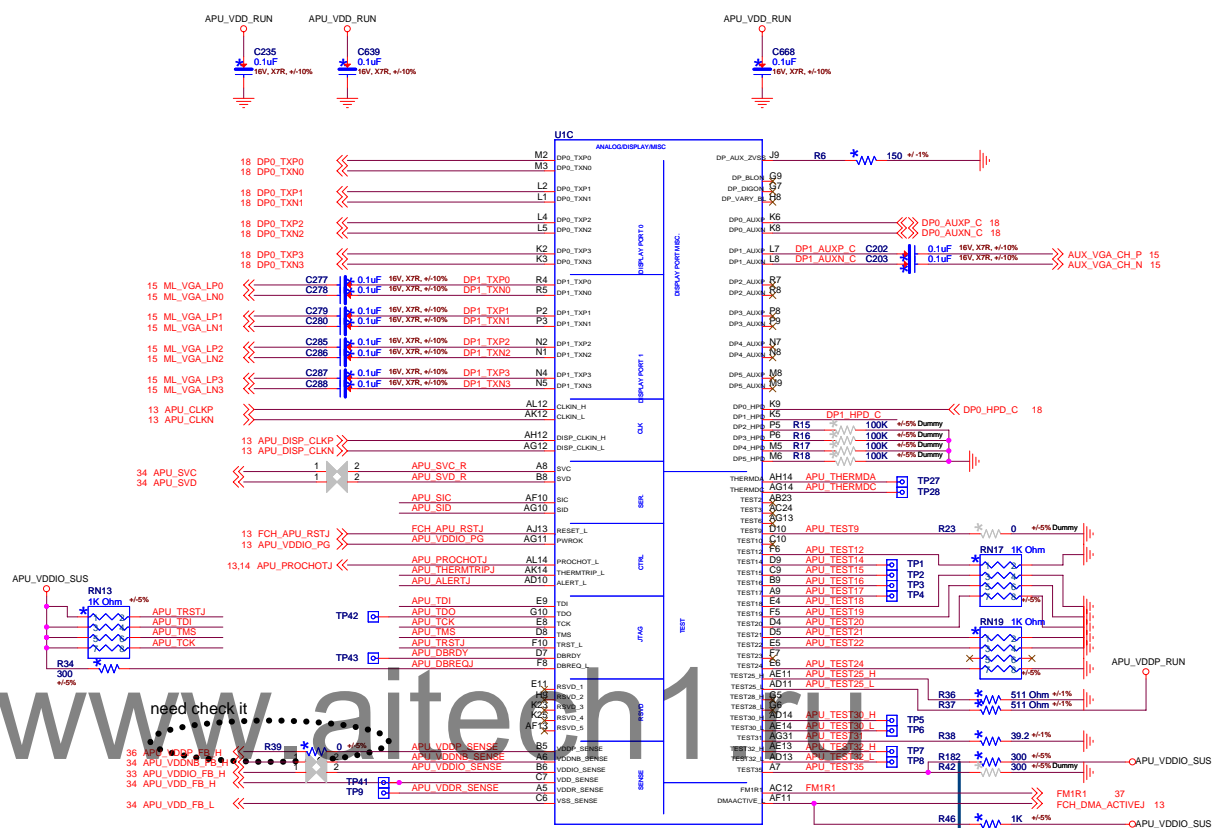


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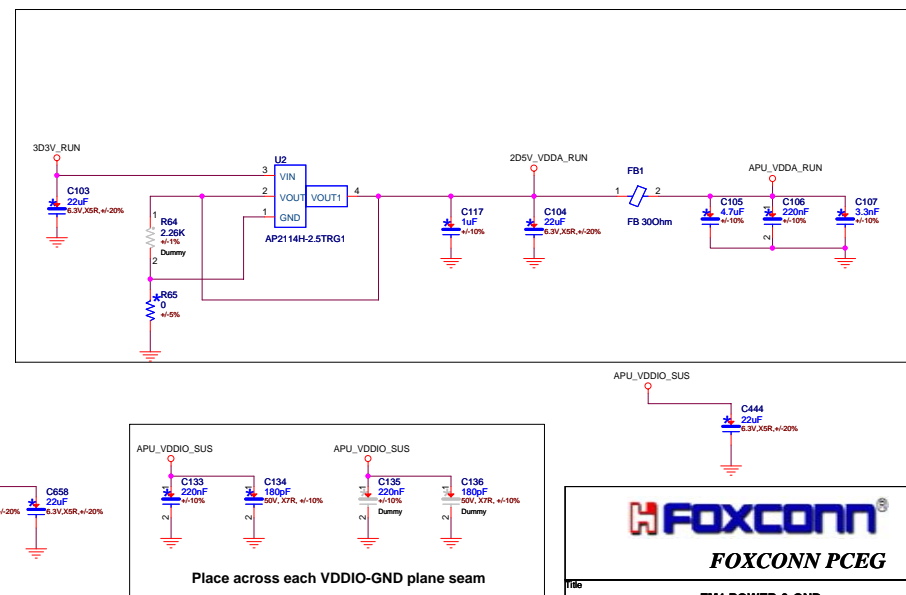
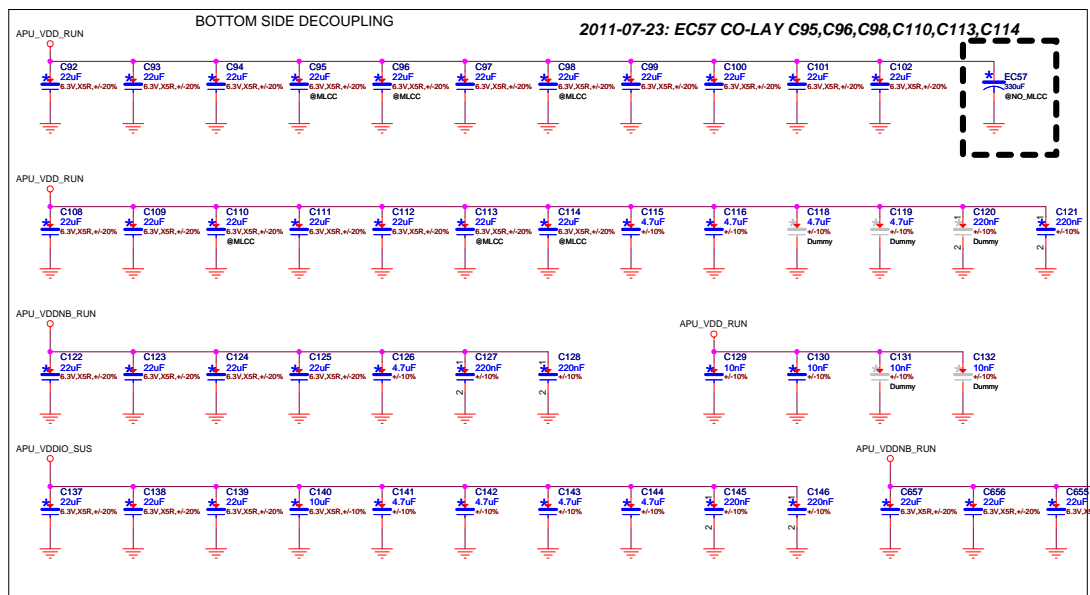
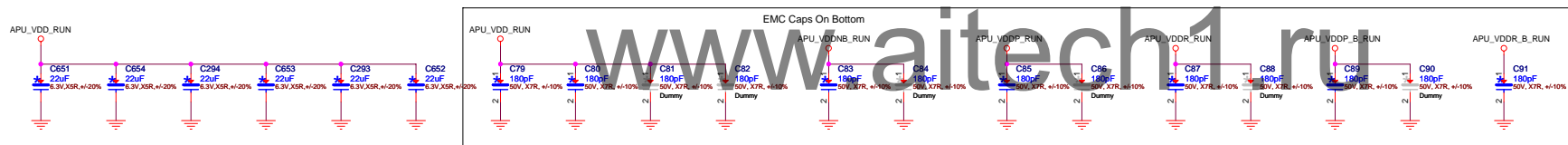
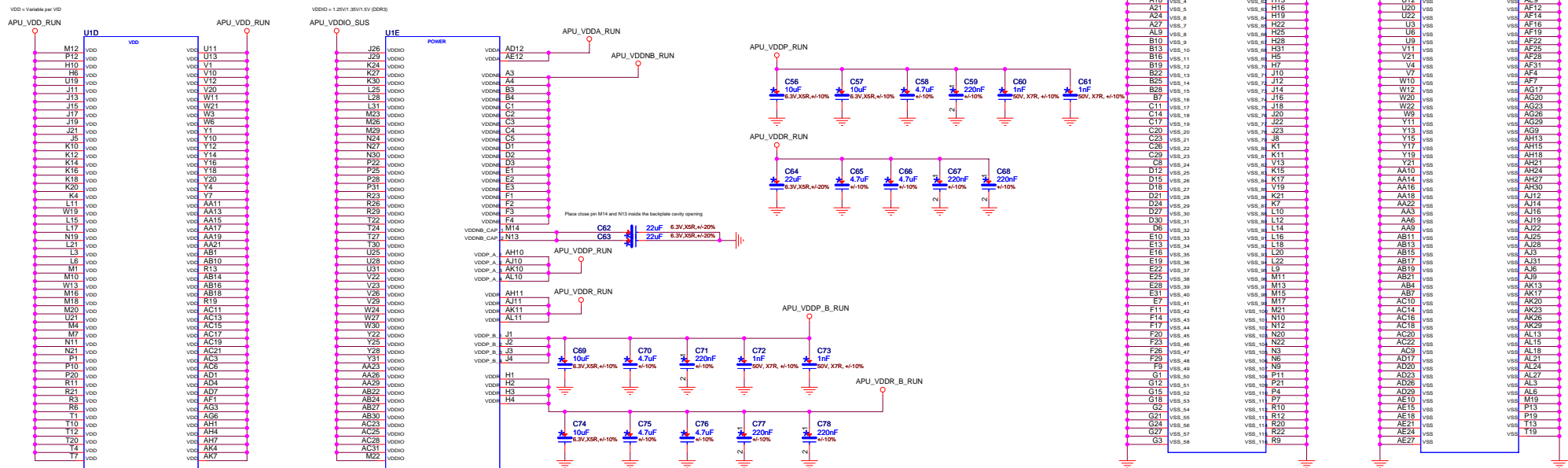


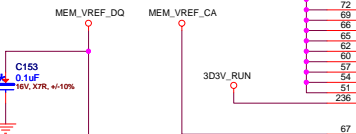
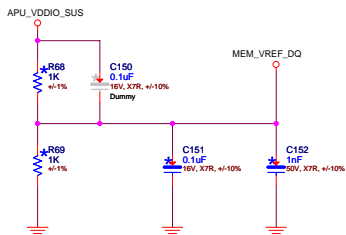
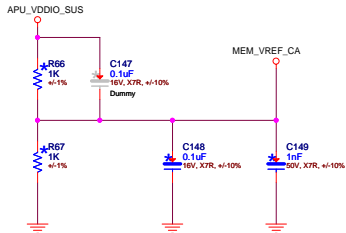
2011-07-07: For ISL6328_POWOK_R Dummy R187, Q7, R207, stuff R43 following CRB



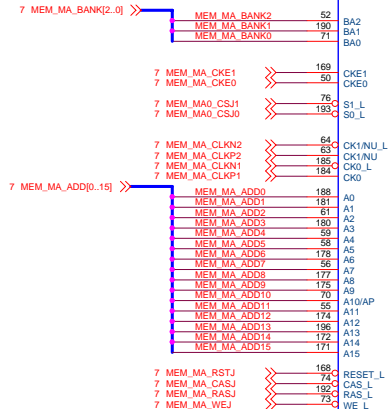
2011-07-07: Change R182 from 1k to 300 ohm

PROCESSOR POWER AND GROUND

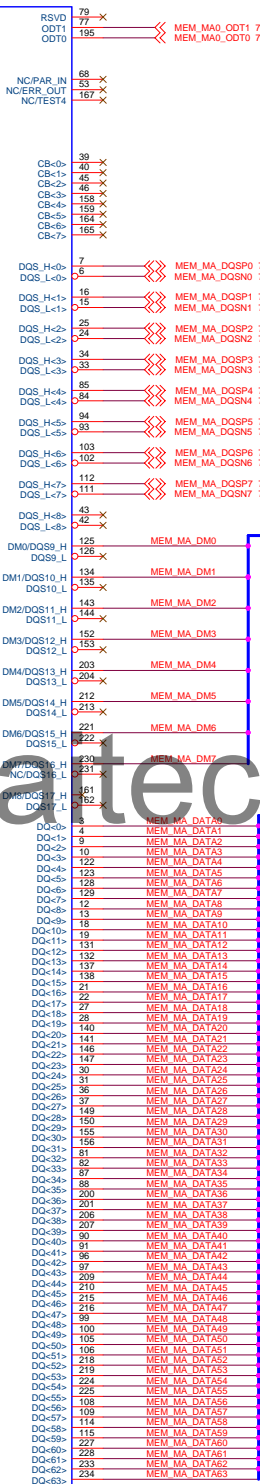




SMBUS 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2



DDR I I

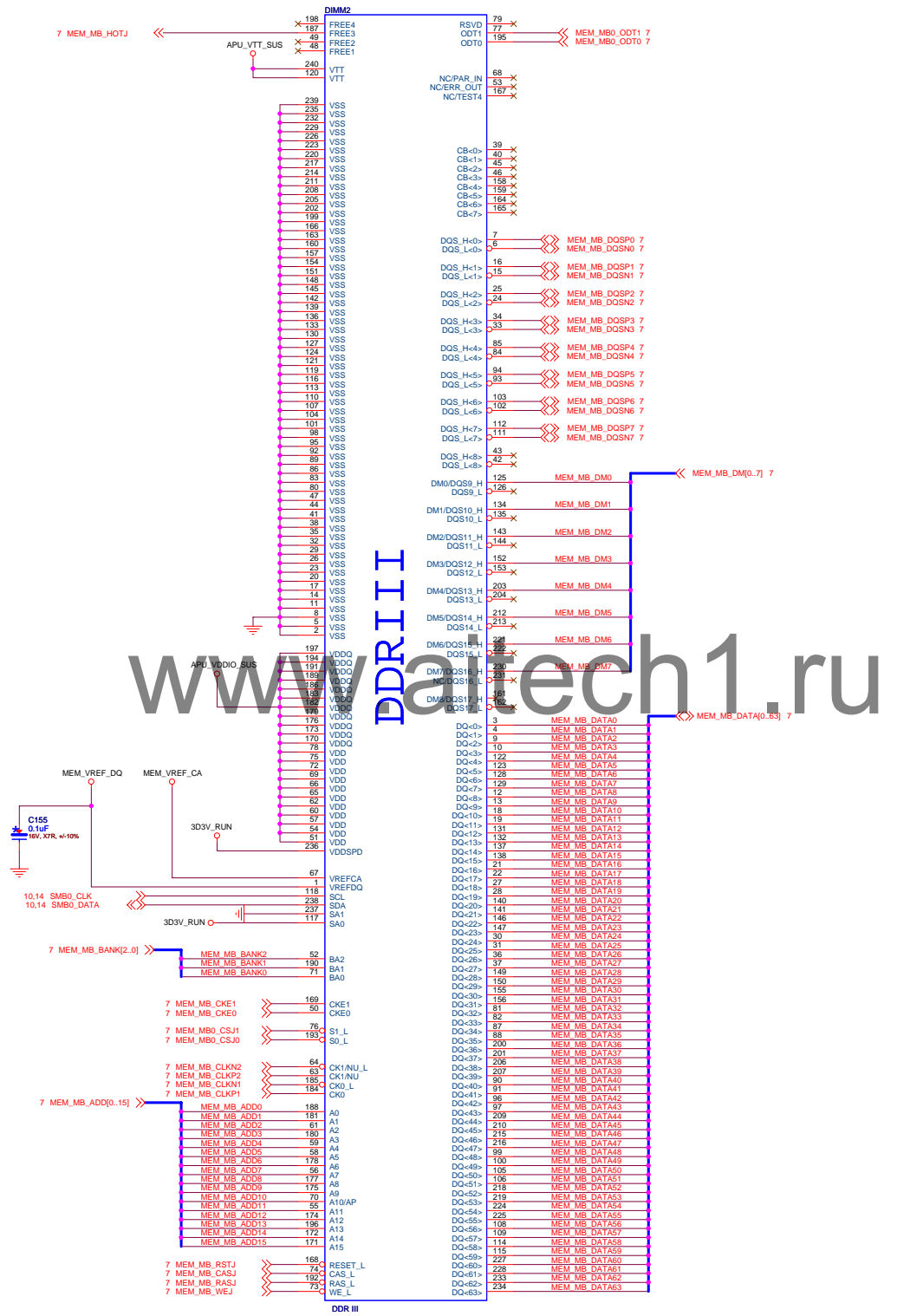


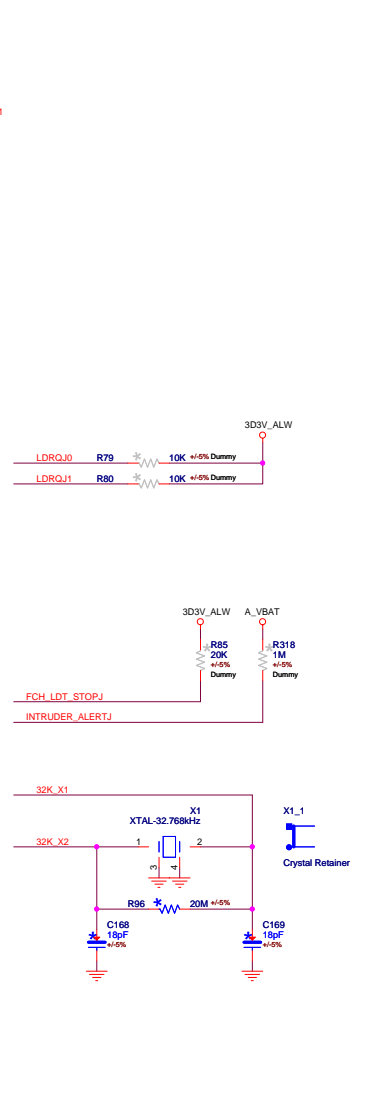
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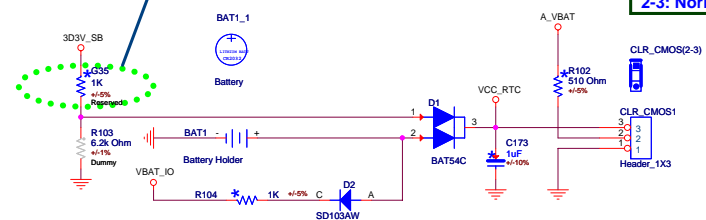
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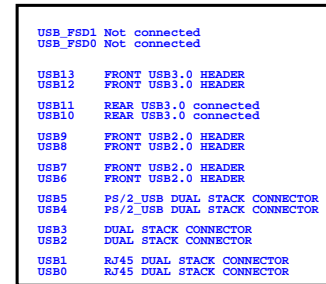


2011-07-25: Change G35 from short pad to 1K resistor for safty test



1-2: Clear COMS
2-3: Normal

<i>FCH_PCIE_RSTJ_GPP FOR APU PCIE DEVICE</i>	PCIE 16X
<i>PCIE_RST2J_GPP FOR FCH PCIE DEVICE</i>	PCIE 1X / LAN
<i>PCIE_ARSTJ FOR LPC DEVICES</i>	SIO

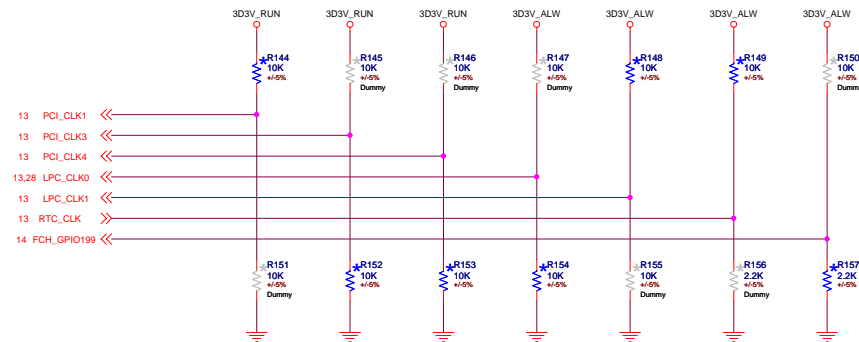


U46

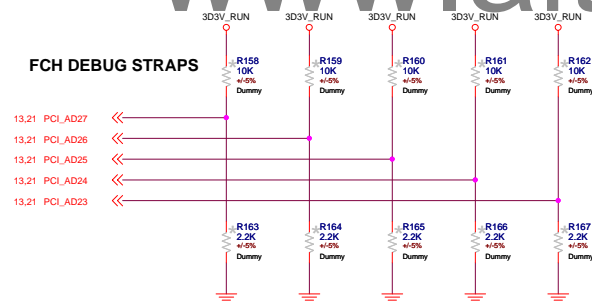
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	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	GPIO199
PULL HIGH	ALLOW PCI-E GEN2	USE DEBIO STRAPS	NON-FUSION APU CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	SS+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM
PULL LOW	FORCE PCI-E GEN1 DEFAULT	IGNORE DEBIO STRAPS DEFAULT	FUSION APU CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SS+ ENABLE	L = SPI ROM DEFAULT



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK termination DEFAULT	USE DEFAULT PCI-E STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	Inverted REFCLK termination	USE REPPROM PCI-E STRAPS	ENABLE PCI MEM BOOT

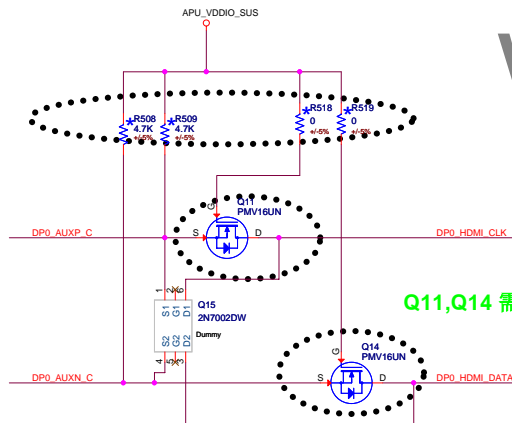
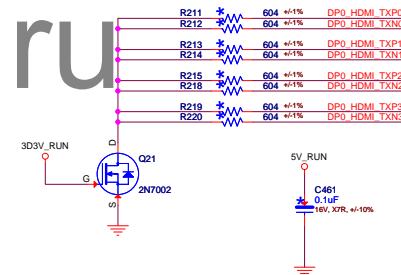
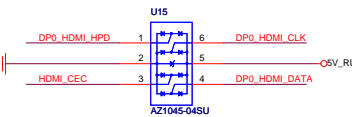
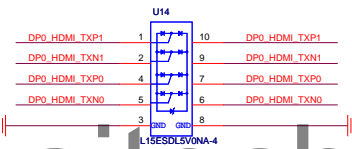
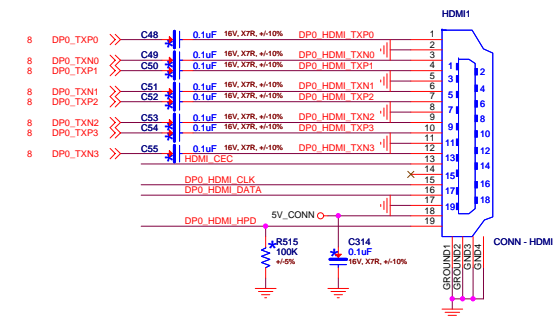
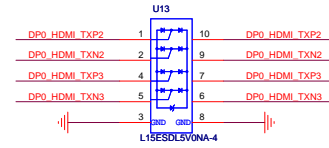
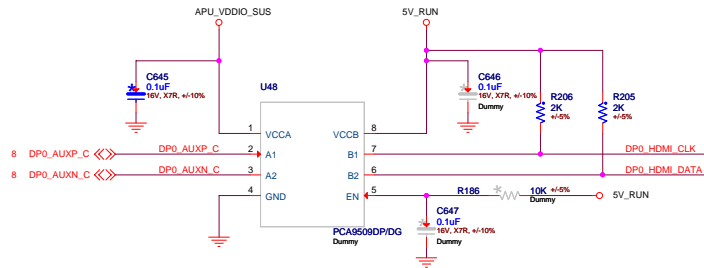
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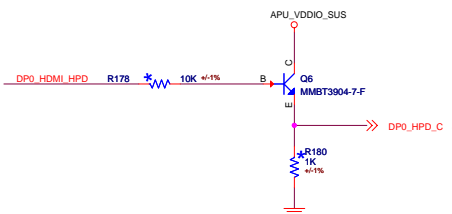
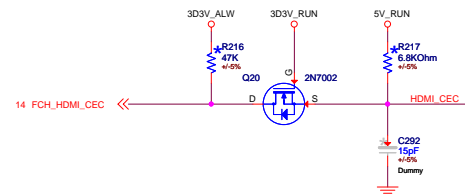
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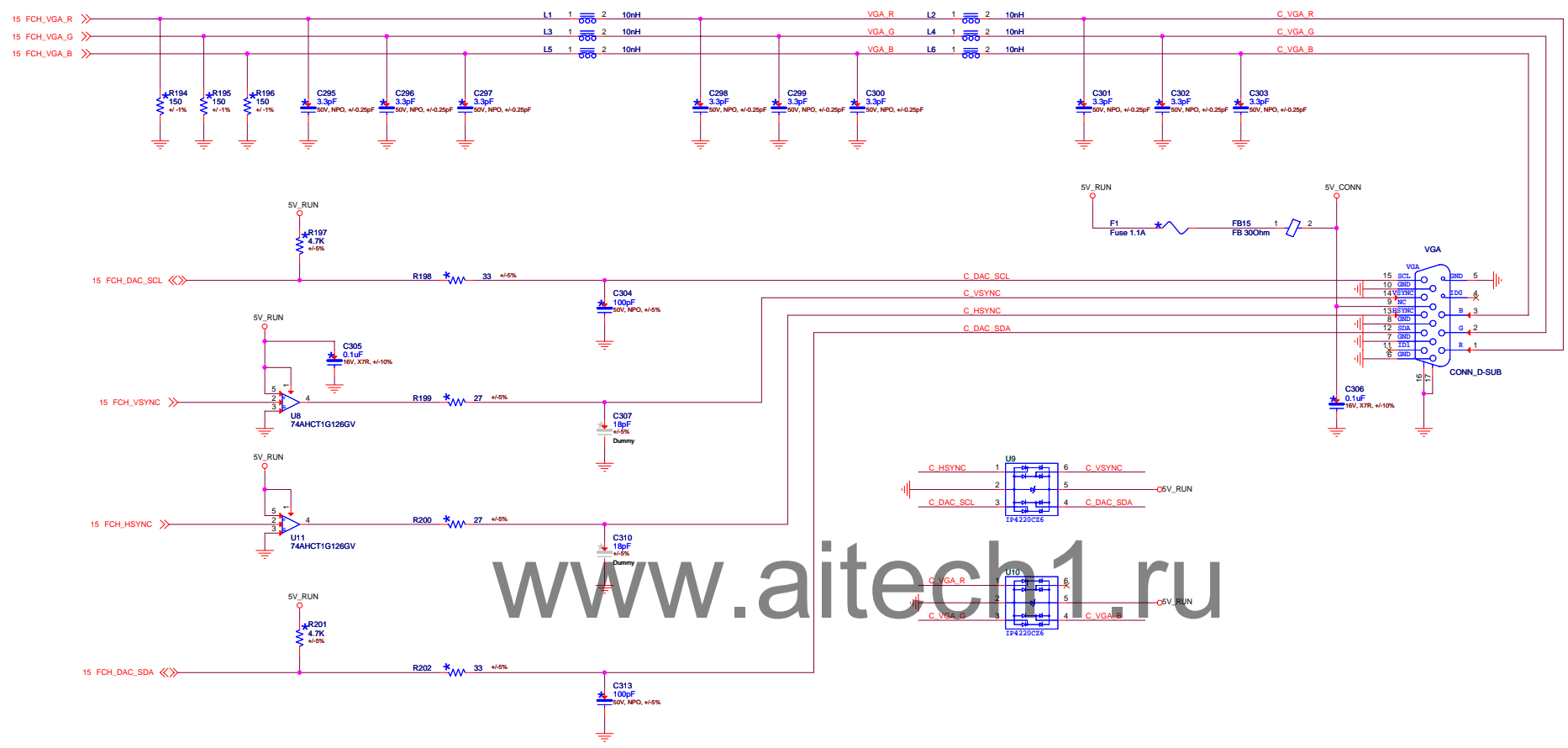
HDMI CONNECTOR

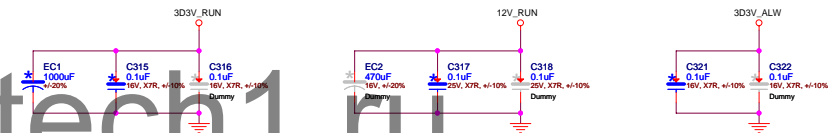
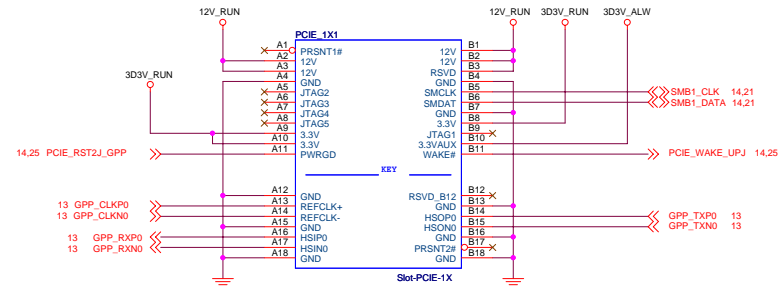
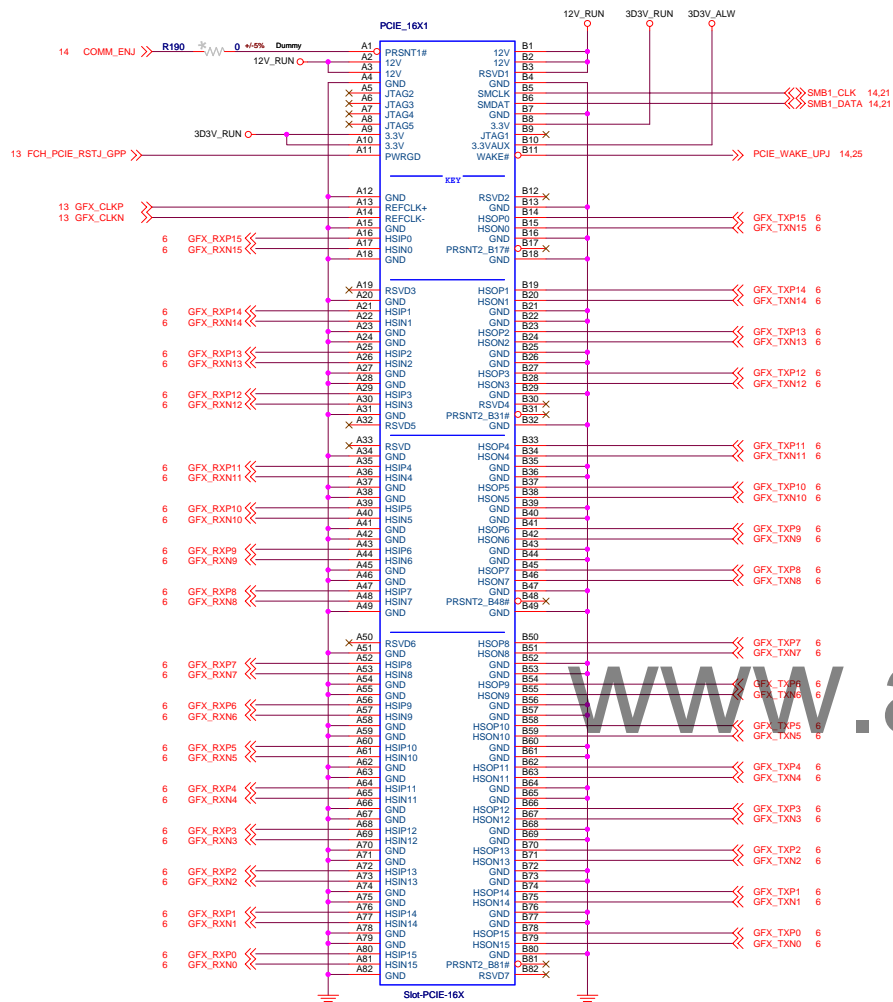


Q11,Q14 需要重新调料



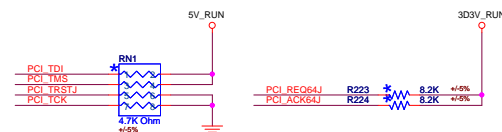
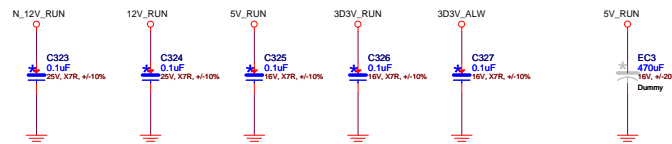
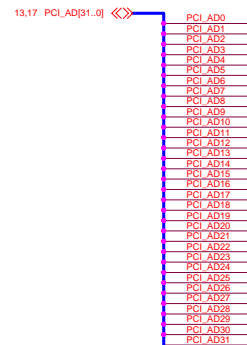
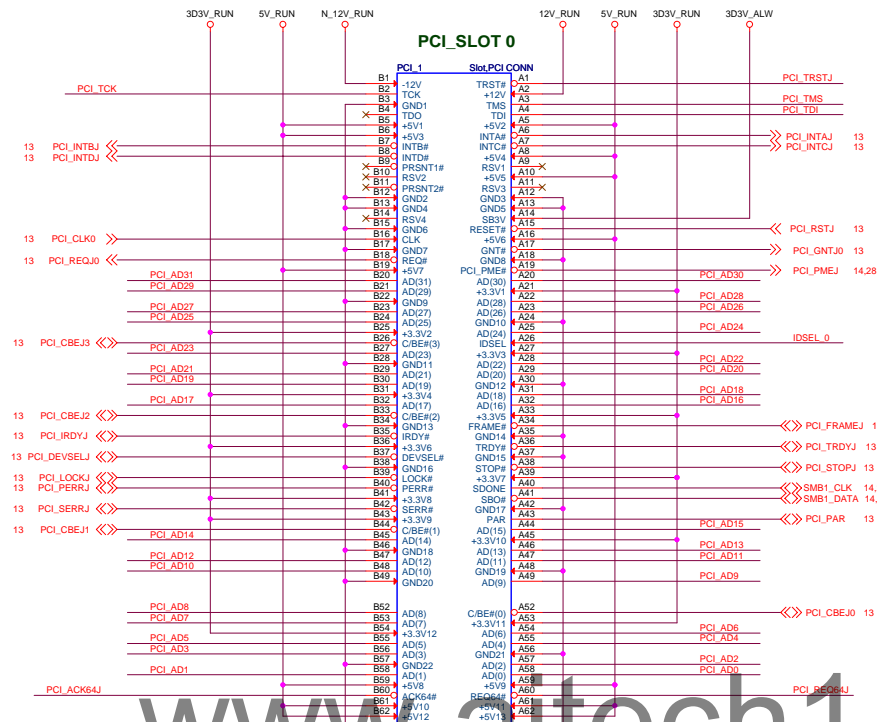
2011-09-01: For fix HDMI can't display issue
1, Change RN21 RESA from 1Kohm to R508,R509(4.7Kohm), R518,R519(0ohm)
2, Change Q11,Q14 from 3904 to PMV16UN





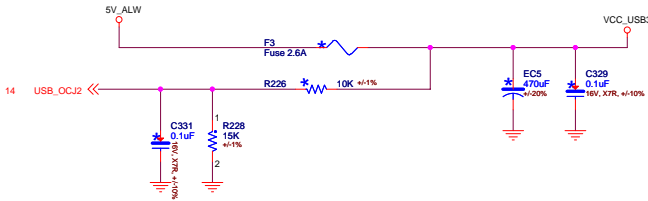
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Title: PCI E X16 & X1 SLOT
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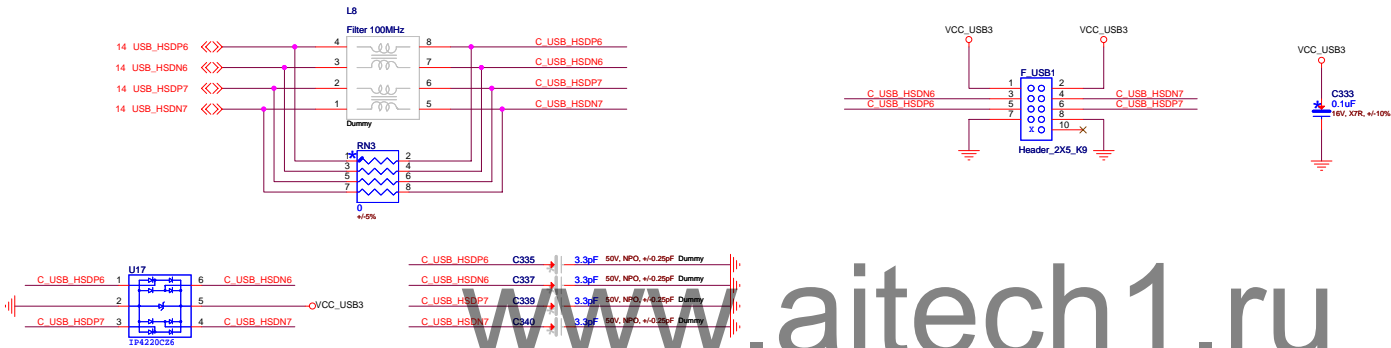


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USB POWER(VCC_USB3) for FUSB1 & FUSB2



FUSB1 (Data 6 & 7)

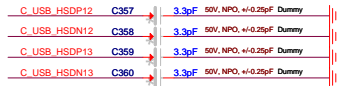
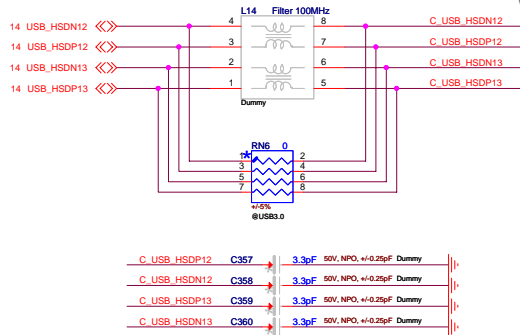
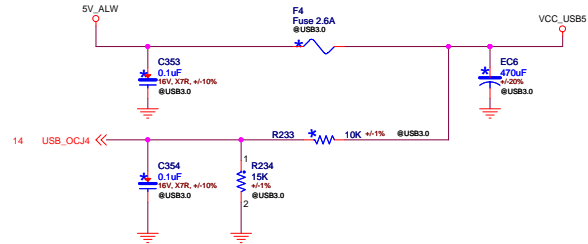


FUSB2 (Data 8 & 9)

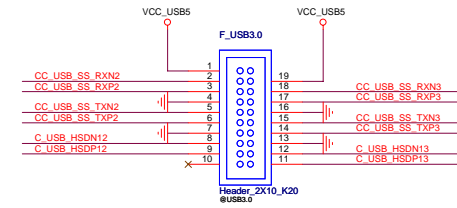
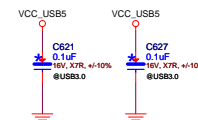
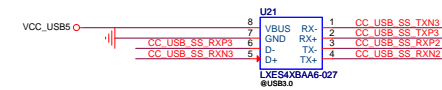
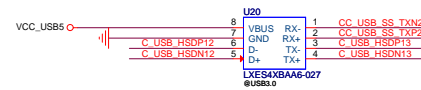
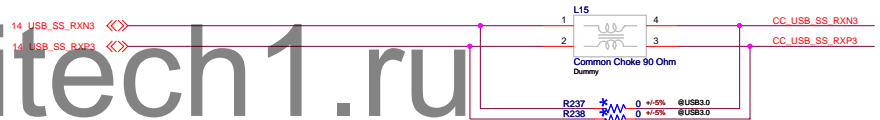
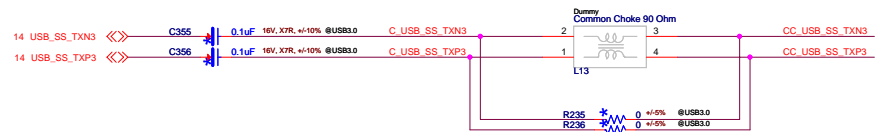
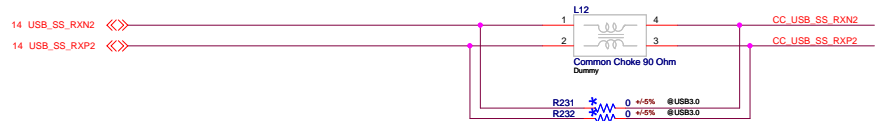
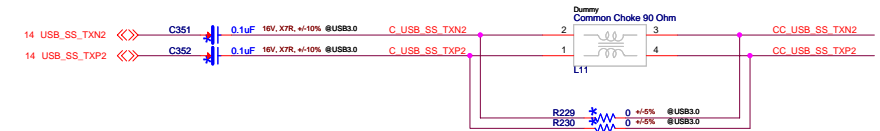


2011-07-27: Delete U18

USB POWER (VCC_USB5) for FUSB3.0



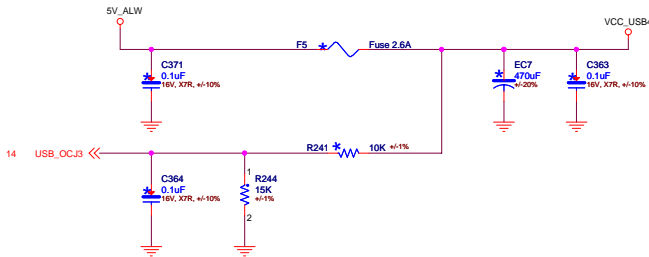
FUSB3.0 (USB3.0 data 2 & 3 / USB2.0 data 12 & 13)



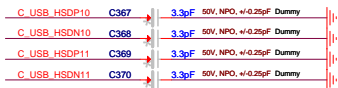
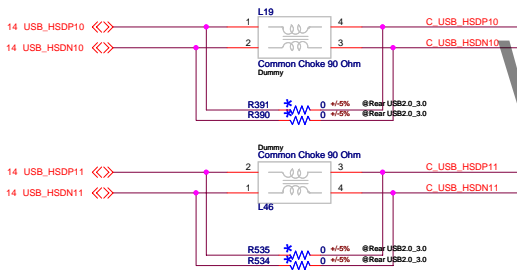
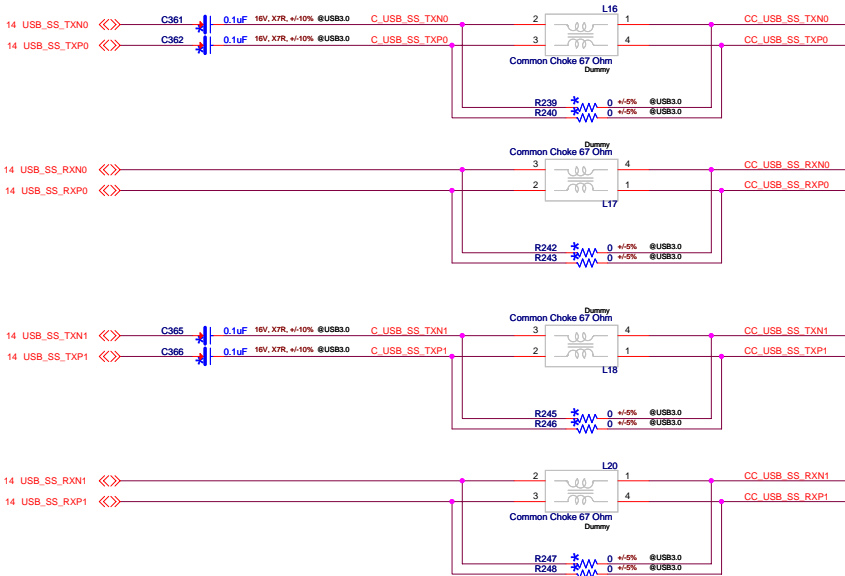
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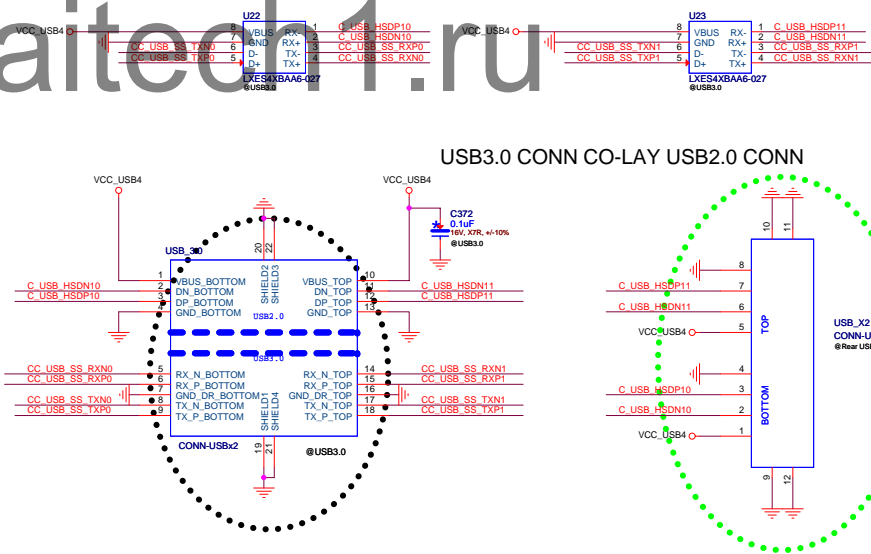
USB POWER (VCC_USB4) for USB3.0 & NIC_USB1



REAR USB3.0 (USB3.0 data 0 & 1 / USB2.0 data 10 & 11)

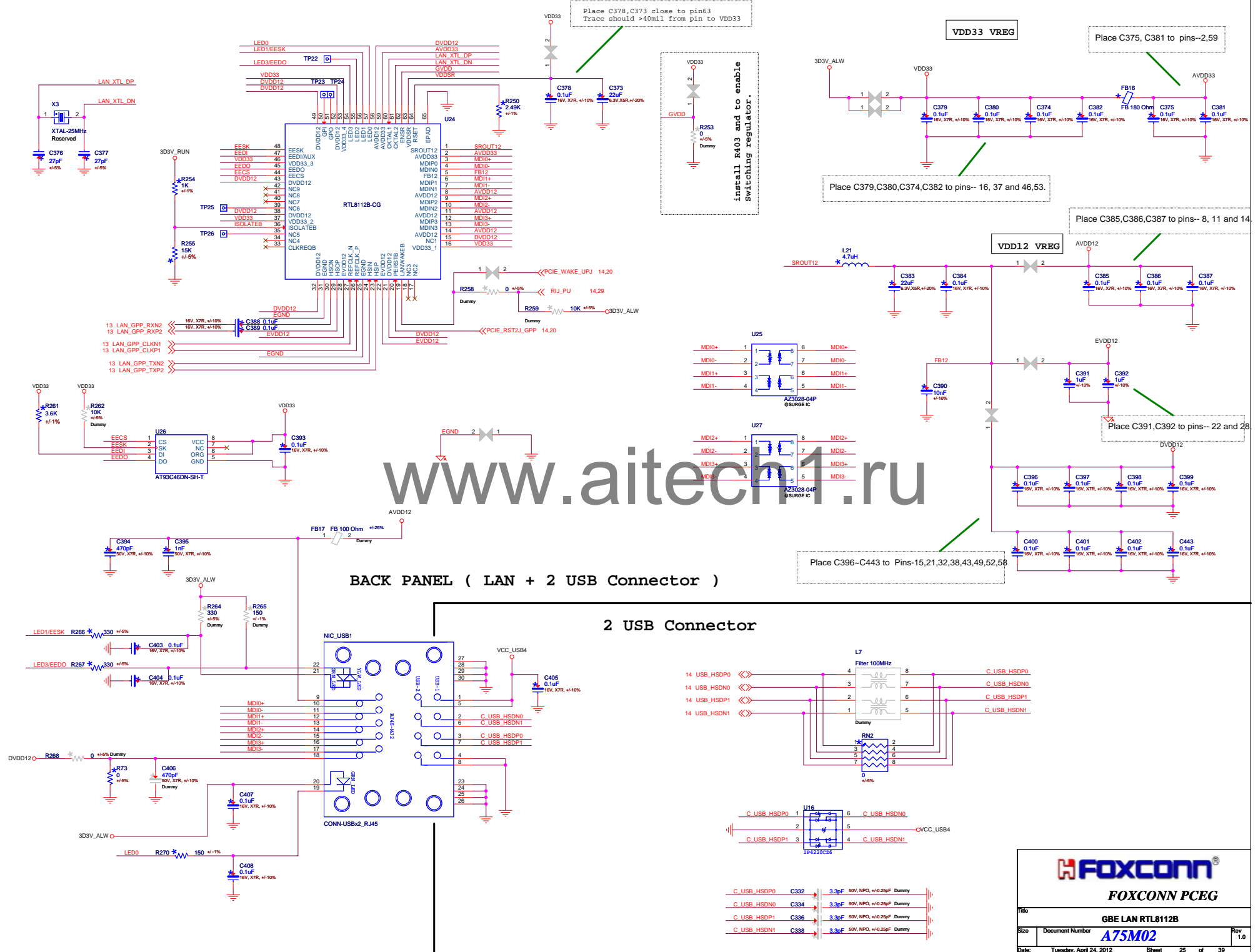


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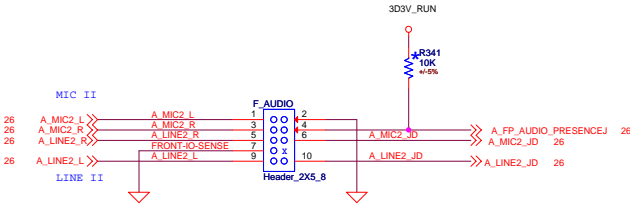


2011-08-31: Change USB3.0 CONN from 34041R400-600-G to 34041QY00-600-G(shorter)

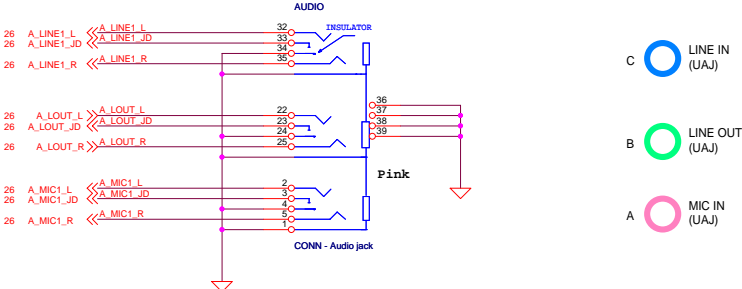
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Front_Audio

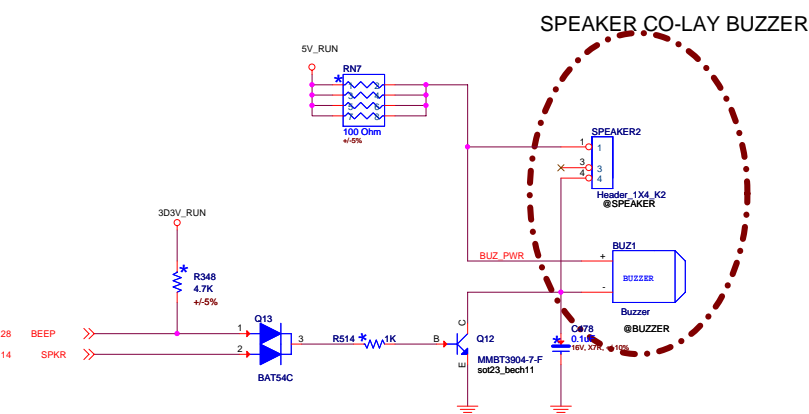


3 PORT Audio Jack



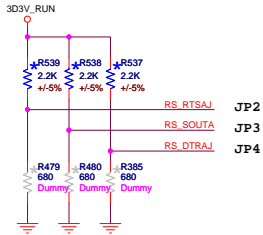
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BUZZER/Speaker Header



Power On Strapping Options

	Symbol	Strapping Event	value	Description
JP2 (Pin 57)	WDT_EN	internal VCC-OK LRESET#	1 0	Disable WDT to reset PWRGD Enable WDT to reset PWRGD
JP4 (Pin 61)	K8PWR_EN	internal VCC-OK	1 0	Disable K8 power sequence function Enable K8 power sequence function
JP3 & JP5 (Pin59&Pin21)	FAN_CTL_SEL	internal VCC-OK	11	The default value of EC index 63h/6Bh/73h is 80h
			10	The default value of EC index 63h/6Bh/73h is FFh
			01	The default value of EC index 63h/6Bh/73h is 00h
			00	The default value of EC index 63h/6Bh/73h is 40h
JP8 (Pin 30)	RSMRST_SEL	internal 3VSB_OK	1	RSMRST# output detected by 3VSB
			0	RSMRST# output detected by SYS_3VSB

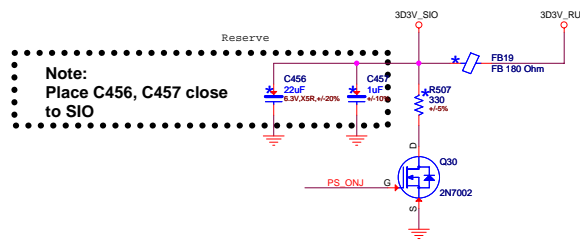
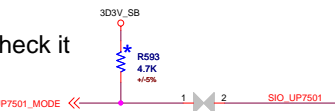
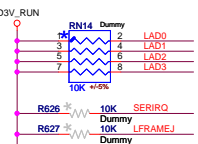
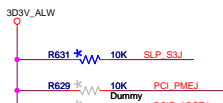


Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

UART1



2011-08-20: exchange SYSFAN_TAC and SYSFAN_CTL



Note:
Place C456, C457 close to SIO

If without use these pins...Please pull-up. Don't let it floating.

1. Pin 6: ATXP0
2. Pin 29: SUSB#
3. Pin 21/ Pin 57/ Pin 59/ Pin 61
4. Pin 37-40 KCLK/KDAT/MCLK/MDAT
5. Pin 63 pull high to 3VSB

Note: use EUP function Pin29/Pin30/Pin31/Pin34/Pin42 pull high to SYS_3VSB. Pin 5, Pin 32, pull high to 3.3VSB. Pin33 pull high to VCCB.

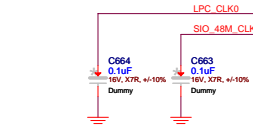
Temperature Sensor
(PECI / SM_LINK CPU temperature set to TMPIN1
SM_LINK PCH temperature set to TMPIN2)

Note:
Place C414 close to SIO, and Do Not remove this 1uF Cap. of VREF.

Note: Don't remove Pin 32 Damping resistor.

Tantalum cap.
(Spare for battery installation glitch)
Layout Note:
*Recommended net "VBAT" minimum trace width 12mils.
*Isolated the SIO's VBAT & ICH's VCCRTC pin

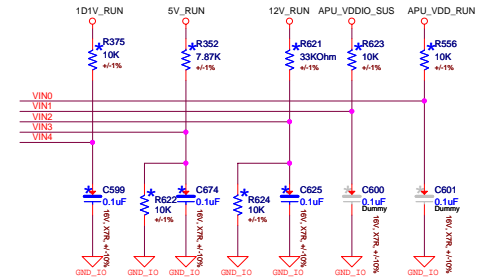
The trace between SIO's CLKIN & oscillator (output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.



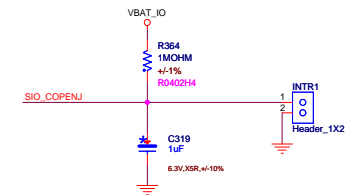
2011-08-11: Change FB10 from FB to GAP for match ITE request



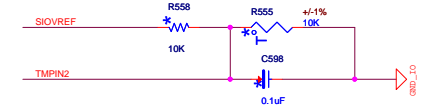
Voltage Monitor



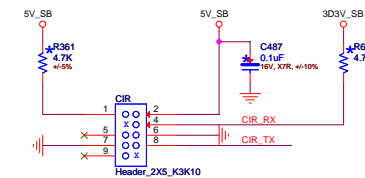
INTRUDE ALERT HEADER



SYSTEM TEMPERATURE



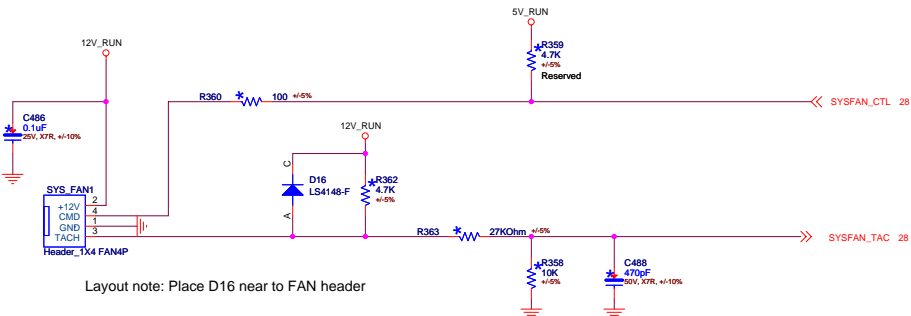
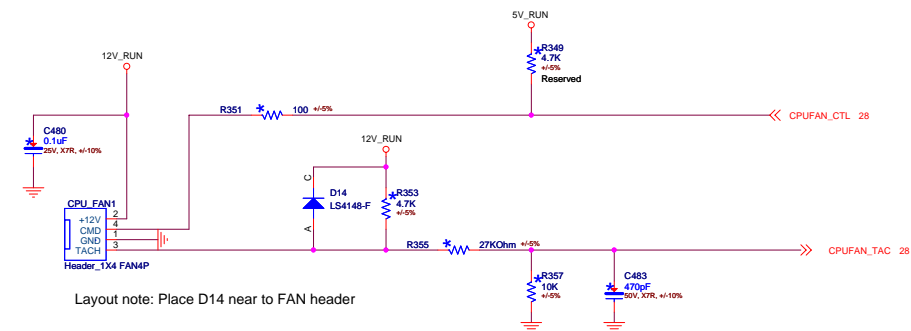
IR/CIR



FOXCONN
FOXCONN PCEG

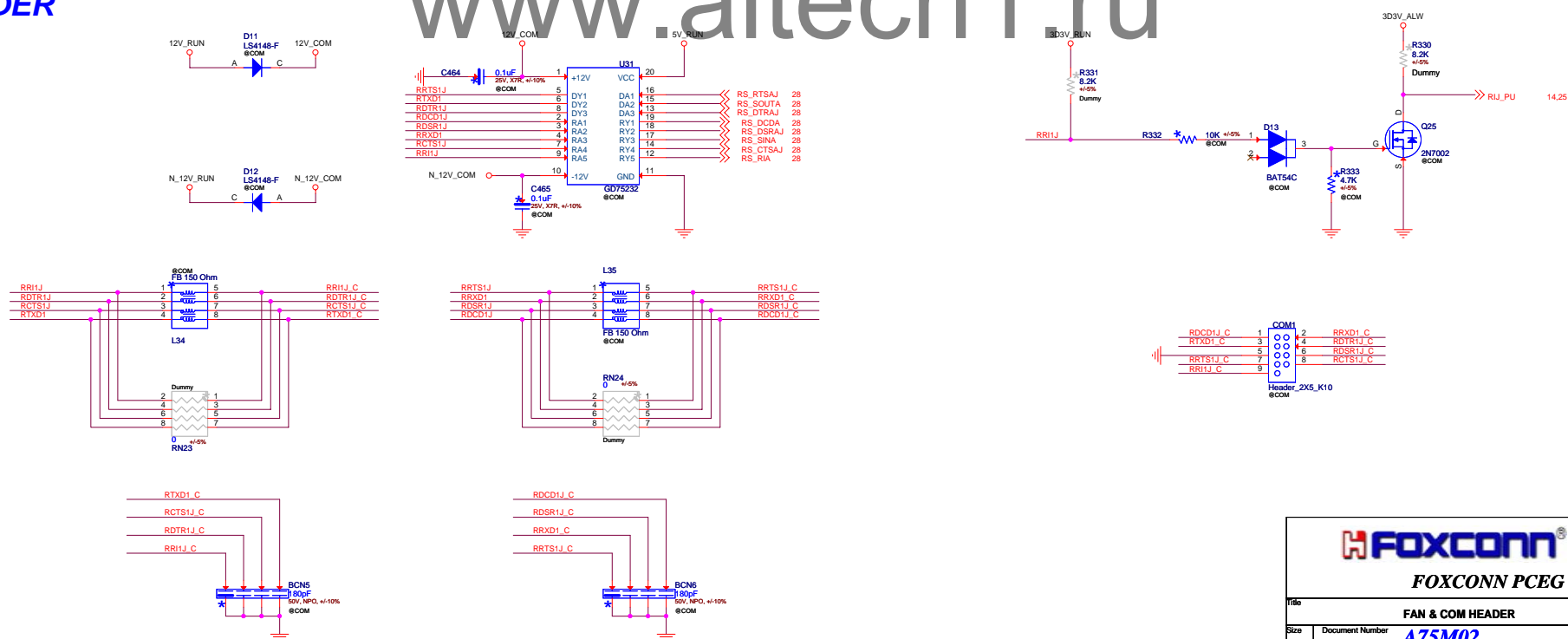
Title	HW MONITOR/CIR & IT8772/ECX
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FAN

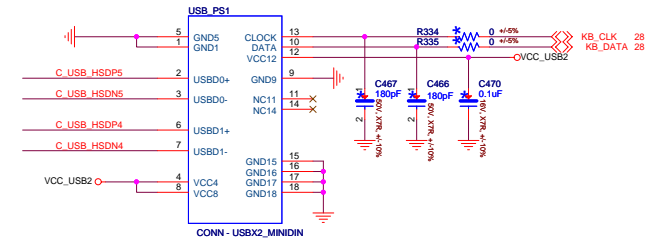


COM HEADER

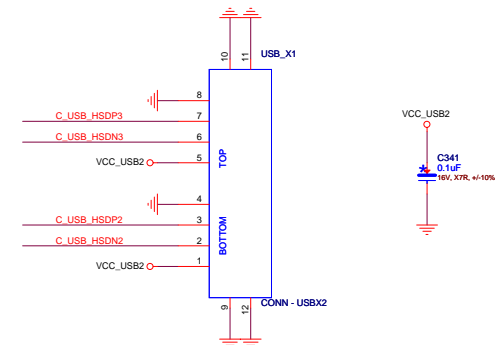
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REAR_USB



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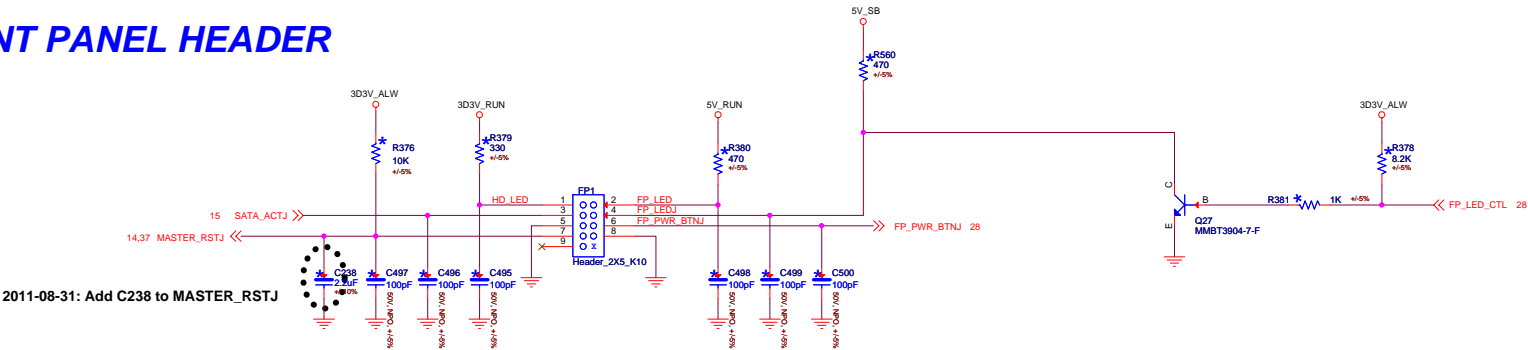


PS2 & REAR USB2.0 CONNECTOR

A75M02

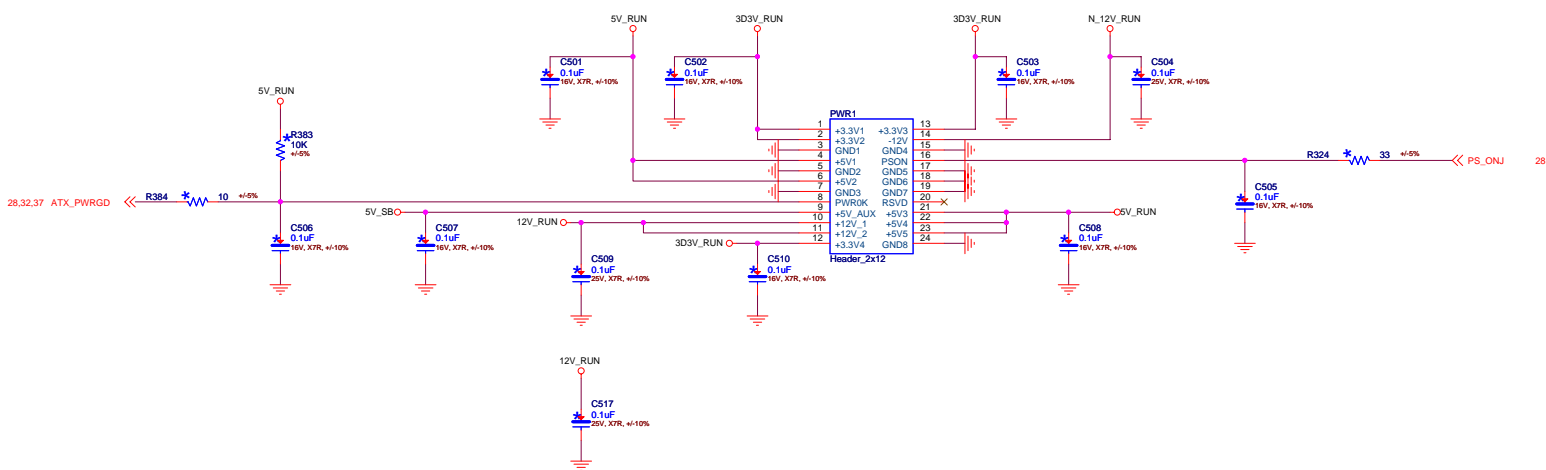
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PS2 & REAR USB2.0 CONNECTOR			
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FRONT PANEL HEADER

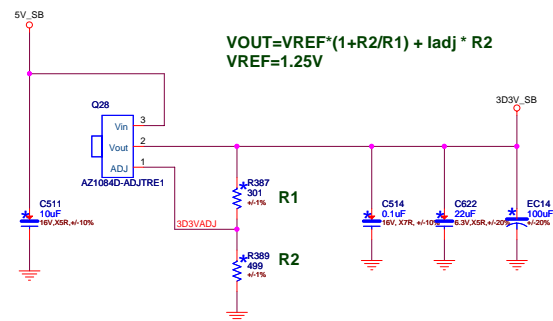


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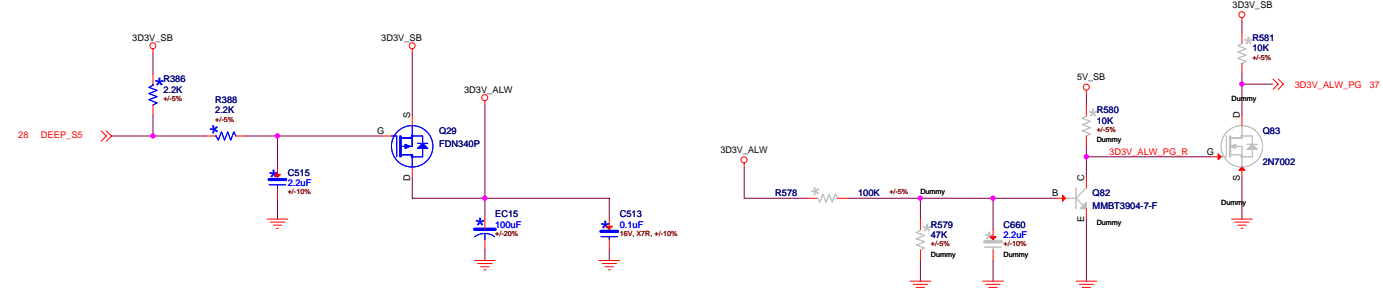
24 PIN ATX CONNECTOR



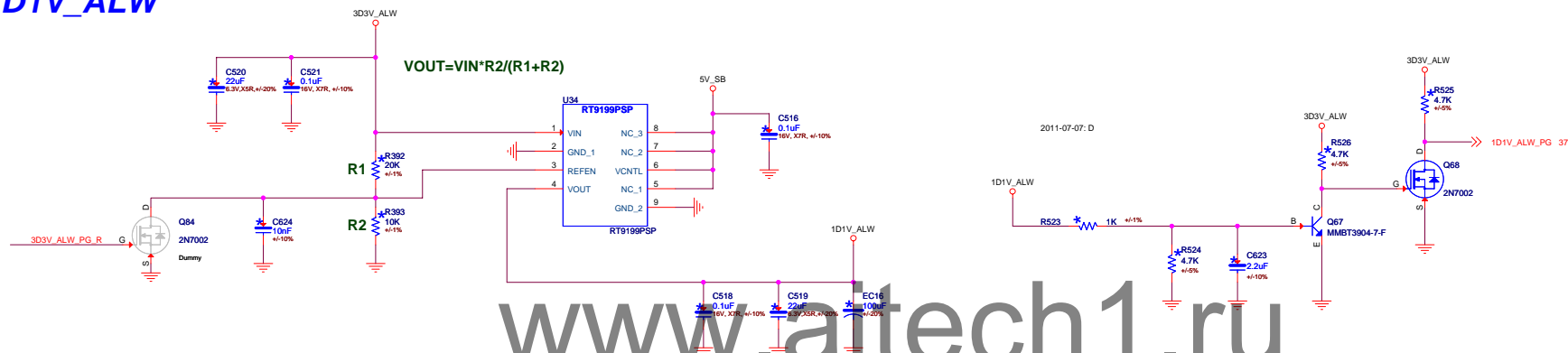
3D3V_SB



3D3V_ALW

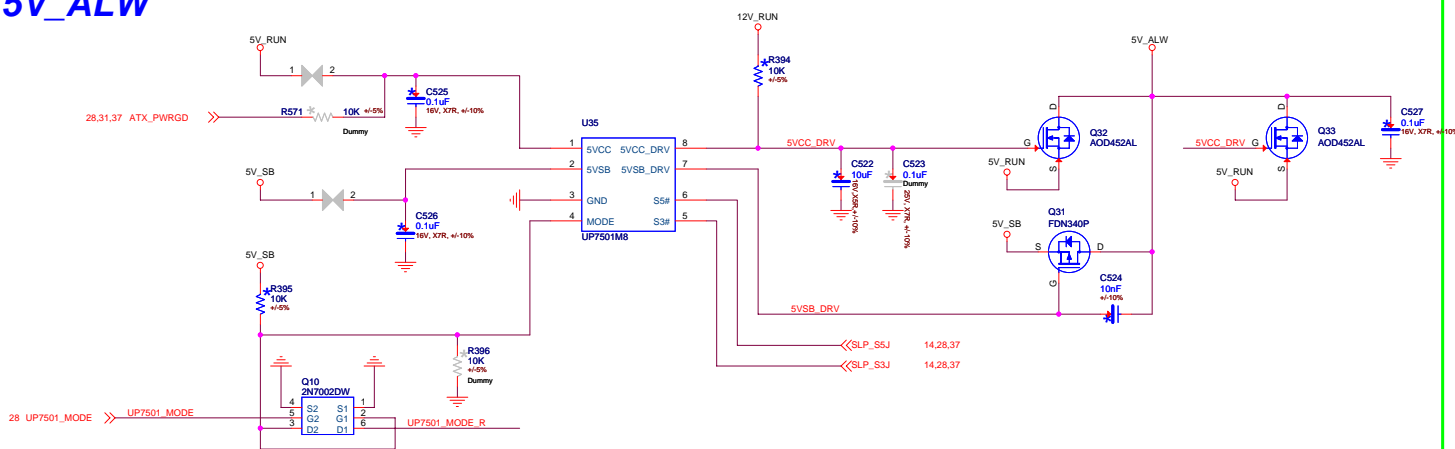


1D1V_ALW

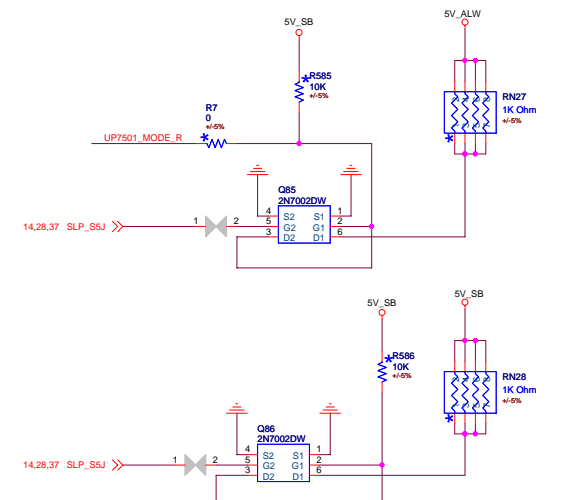


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5V_ALW



S5#	S3#	MODE	5V_ALW
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown



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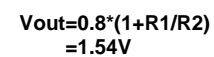
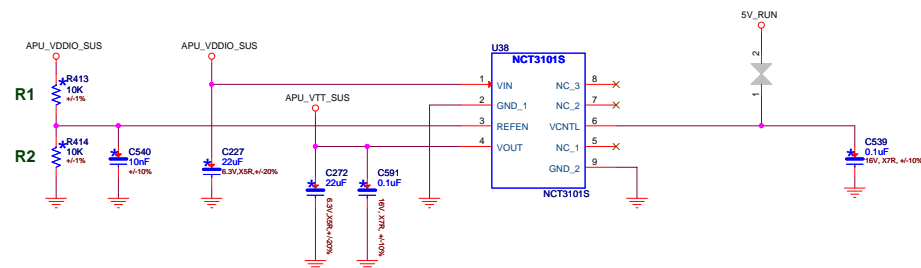
FOXCONN PCEG

PWR MAIN & OTHER POWERS

A75M02

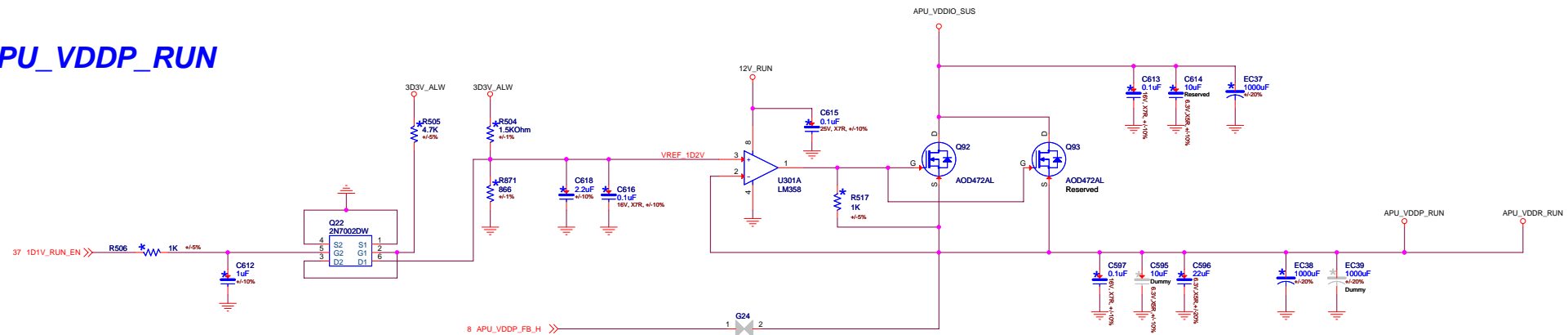
Title: _____
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2011-08-11: Change EC19,EC35 from 16V 270uf to 6.3V 470uf to slove Pin too close to board edge


$$V_{OUT} = V_{IN} \cdot R_2 / (R_1 + R_2)$$


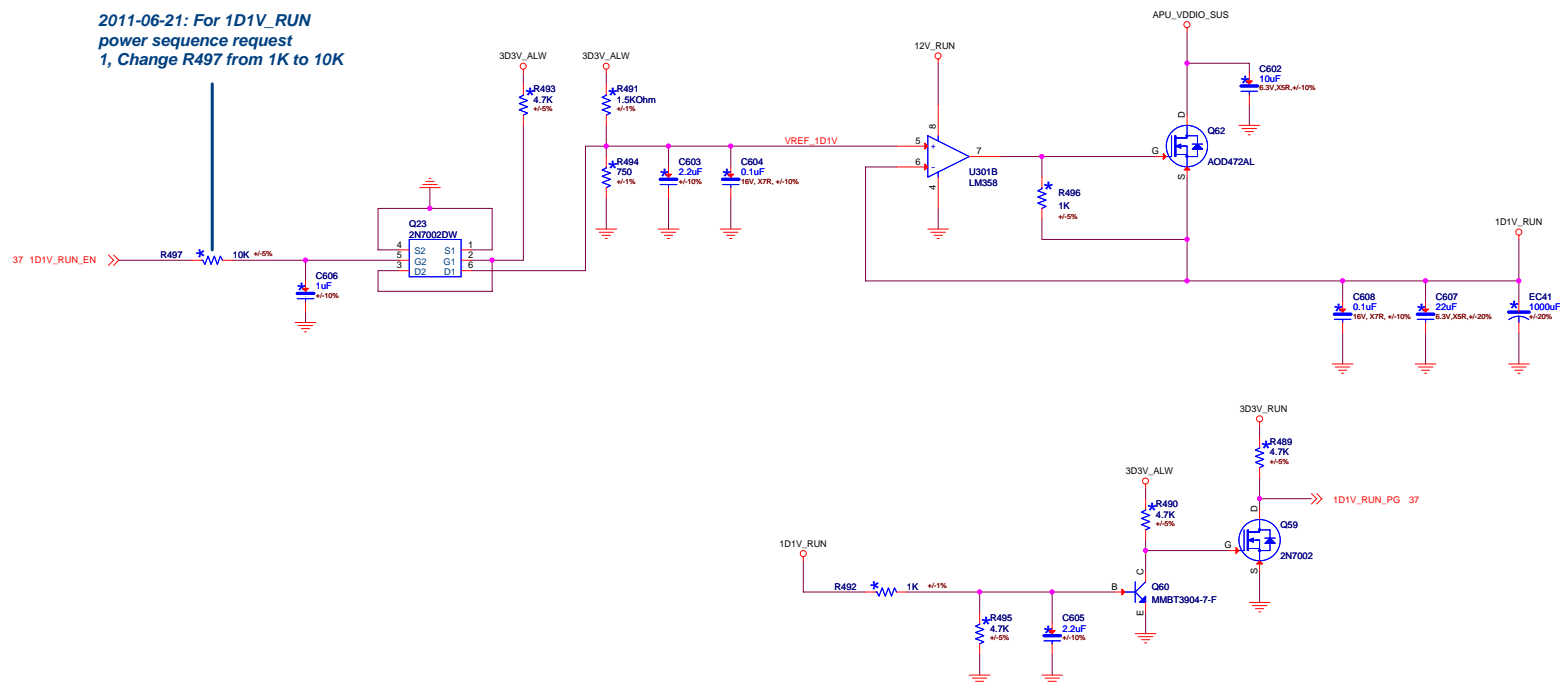


APU_VDDP_RUN

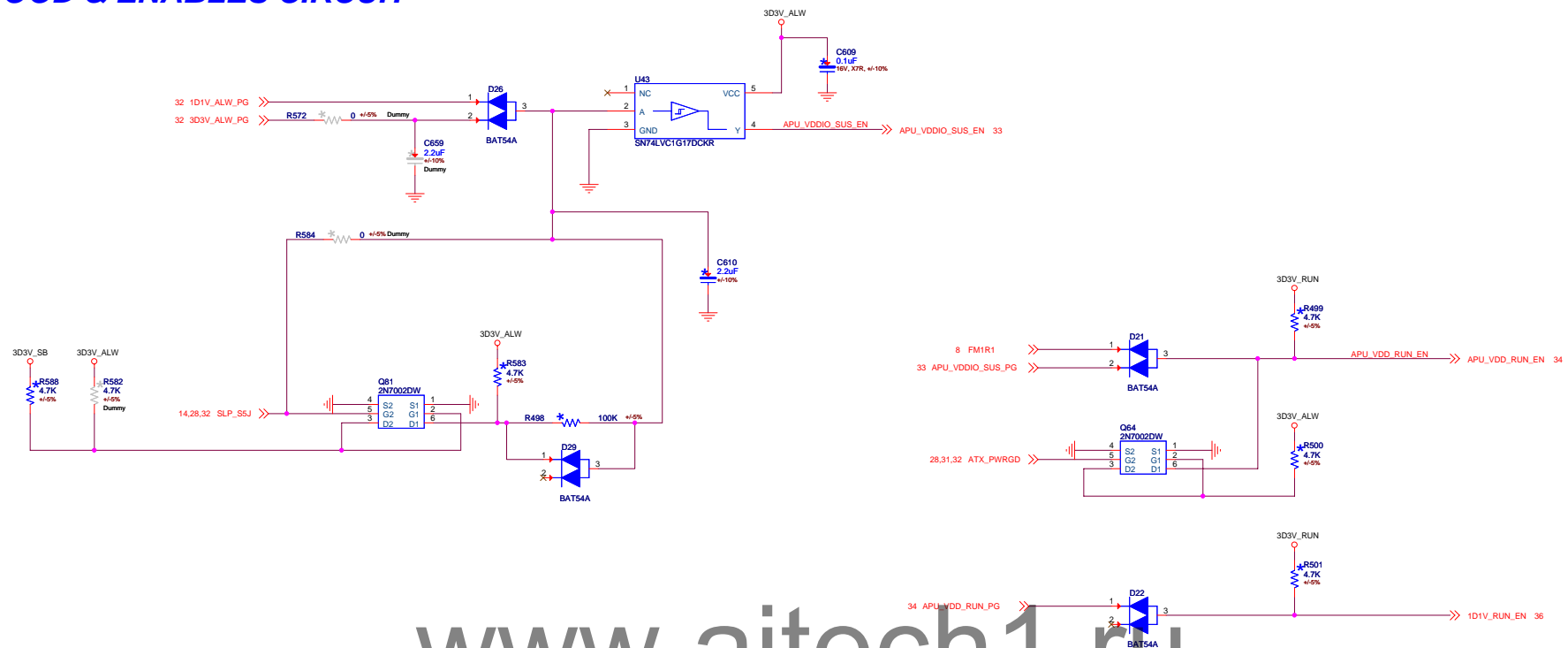


1D1V_RUN

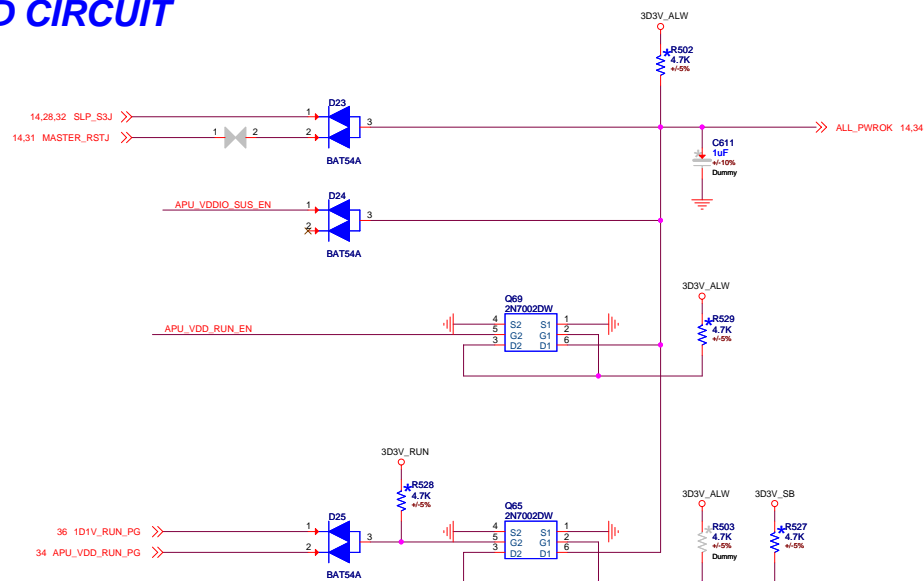
**2011-06-21: For 1D1V_RUN
power sequence request
1, Change R497 from 1K to 10K**

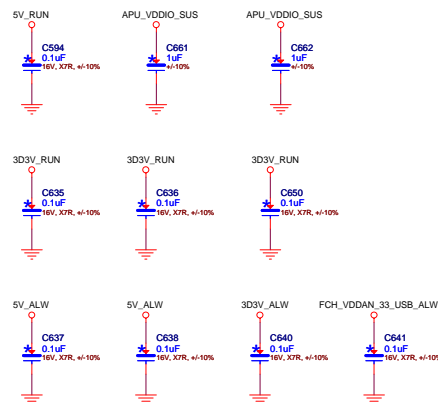
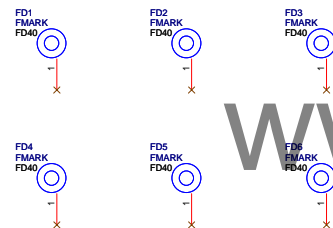
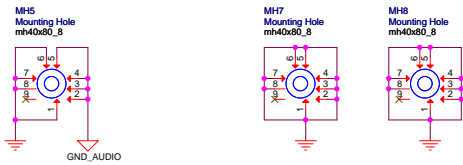
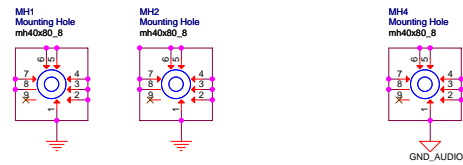


POWER GOOD & ENABLES CIRCUIT



ALL POWER GOOD CIRCUIT





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FAB A-FAB 1.0

2011-08-11

- 1, Change EC19,EC35 from 16V 270uf to 6.3V 470uf to slove Pin too close to board edge, and Dummy EC19 (270uF 16V SP-CAP \$0.072, 470uF 6.3V SP-CAP \$0.0654)
- 2, Change FB10 from FB to GAP for match ITE request
- 3, 2011-08-20: exchange SYSFAN_TAC and SYSFAN_CTL
- 4, 2011-08-20: Change R99 from 0 ohm to 10 ohm to fix can't power on or power on slowly issue

2011-08-31

- 5: Add C238 to MASTER_RSTJ
- 6: APU_VDDIO_SUS Dummy EC22
- 7: Change USB3.0 CONN from 34041R400-600-G to 34041QY00-600-G(shorter) (price is the same \$0.38)
- 8: Dummy R7,R585,Q85,RN27,Q86,RN28,R586

2011-09-01

- 2011-09-01: For fix HDMI can't display issue
 - 1, Change RN21 RESA from 1Kohm to R508,R509(4.7Kohm), R518,R519(0ohm)
 - 2, Change Q11,Q14 from 3904 to PMV16UN

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Title		
CHANGE HISTORY		
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